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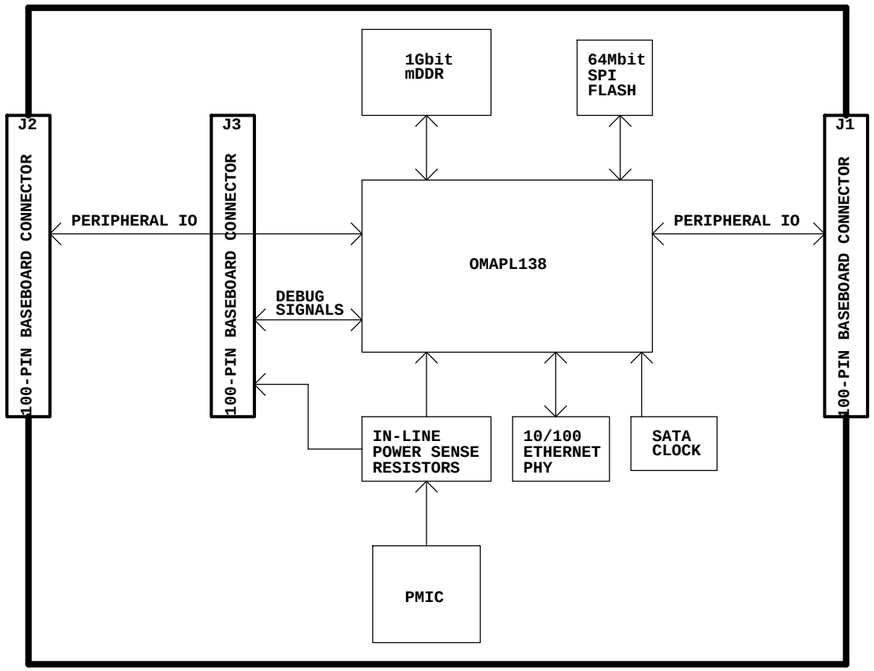
SYSTEM BLOCK DIAGRAM



IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in red are critical, and must be understood and followed.

I2C ADDRESSING

FUNCTION	DEVICE	ADDRESS	I2C BUS
PMIC	TPS65070	100 1000	PROC I2C0
5V IN	INA219	100 0000	PMDC I2C
PMIC 3.3V SW	INA219	100 0001	PMDC I2C
PMIC 1.8V/3.3V SW	INA219	100 0010	PMDC I2C
PMIC 1.2V SW	INA219	100 0011	PMDC I2C
PMIC 1.2V LDO	INA219	100 0100	PMDC I2C
PMIC 1.8V LDO	INA219	100 0101	PMDC I2C
RTC 1.2V LDO	INA219	100 0110	PMDC I2C

IMPORTANT NOTICE:

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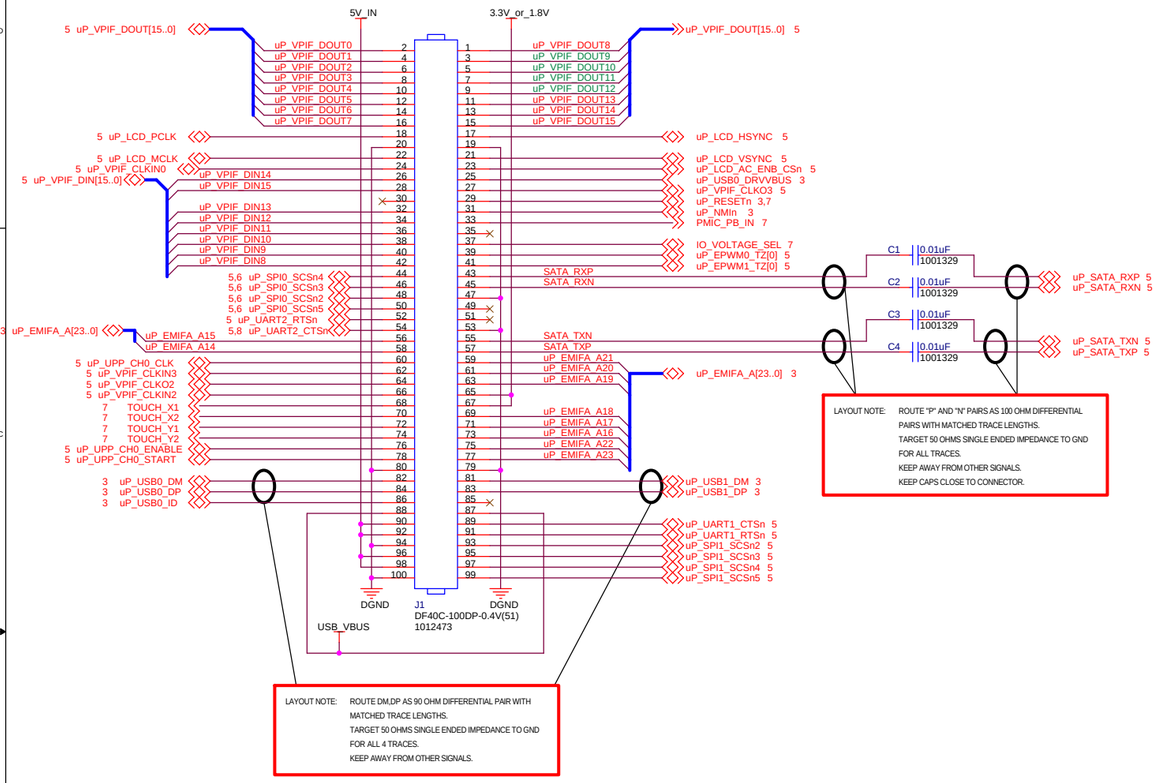
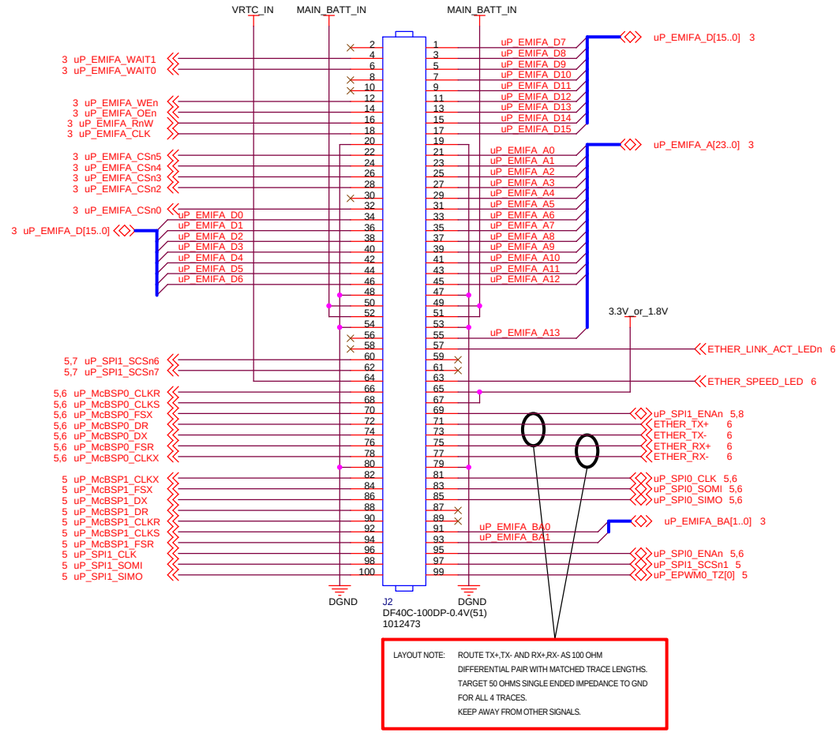
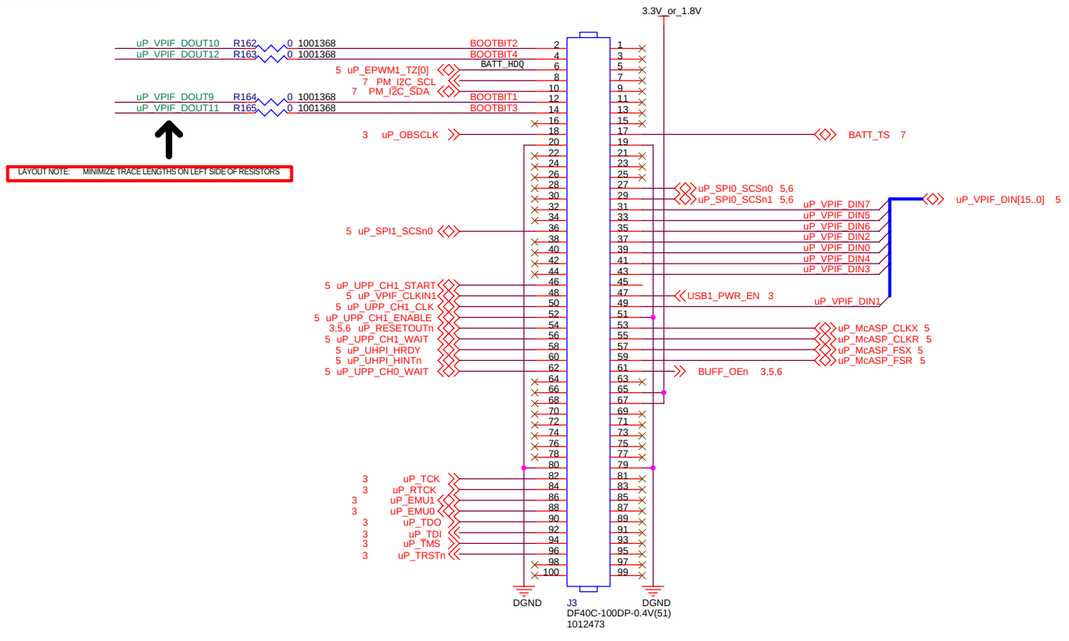
02 - BASEBOARD CONNECTORS







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Title OMAP-L138/C6748/AM1808 SOM-M1		Project PwrMeas	
Number 1015115	Friday, September 24, 2010	Rev C	Sheet 2 Of 9

03 - OMAP MEMORY IF

U1A
OMAP-L138/C6748/AM1808
1012614

2 uP_EMIFA_A[23..0]
2 uP_EMIFA_BA[1..0]
2 uP_EMIFA_D[15..0]
2 uP_EMIFA_CLK
2,5,6 BUFF_OEn
3.3V_or_1.8V

uP_EMIFA_BA0
LCD_PANEL_PWR
R167 1.0K 1% 1006388
DGND

R3 22 5% 1001374

uP_EMIFA_A23	F9	EMA_A_23 / MMCSD0_CLK / GPIO4[7]
uP_EMIFA_A22	A10	EMA_A_22 / MMCSD0_CMD / GPIO4[6]
uP_EMIFA_A21	B10	EMA_A_21 / MMCSD0_D0 / GPIO4[5]
uP_EMIFA_A20	A11	EMA_A_20 / MMCSD0_D1 / GPIO4[4]
uP_EMIFA_A19	C10	EMA_A_19 / MMCSD0_D2 / GPIO4[3]
uP_EMIFA_A18	E11	EMA_A_18 / MMCSD0_D3 / GPIO4[2]
uP_EMIFA_A17	B11	EMA_A_17 / MMCSD0_D4 / GPIO4[1]
uP_EMIFA_A16	E12	EMA_A_16 / MMCSD0_D5 / GPIO4[0]
uP_EMIFA_A15	C11	EMA_A_15 / MMCSD0_D6 / GPIO5[15]
uP_EMIFA_A14	A12	EMA_A_14 / MMCSD0_D7 / GPIO5[14]
uP_EMIFA_A13	D11	EMA_A_13 / GPIO5[13]
uP_EMIFA_A12	D13	EMA_A_12 / GPIO5[12]
uP_EMIFA_A11	B12	EMA_A_11 / GPIO5[11]
uP_EMIFA_A10	C12	EMA_A_10 / GPIO5[10]
uP_EMIFA_A9	D12	EMA_A_9 / GPIO5[9]
uP_EMIFA_A8	A13	EMA_A_8 / GPIO5[8]
uP_EMIFA_A7	B13	EMA_A_7 / GPIO5[7]
uP_EMIFA_A6	E13	EMA_A_6 / GPIO5[6]
uP_EMIFA_A5	C13	EMA_A_5 / GPIO5[5]
uP_EMIFA_A4	A14	EMA_A_4 / GPIO5[4]
uP_EMIFA_A3	D14	EMA_A_3 / GPIO5[3]
uP_EMIFA_A2	B14	EMA_A_2 / GPIO5[2]
uP_EMIFA_A1	D15	EMA_A_1 / GPIO5[1]
uP_EMIFA_A0	C14	EMA_A_0 / GPIO5[0]
uP_EMIFA_BA1	A15	EMA_BA_1 / GPIO2[9]
uP_EMIFA_BA0	C15	EMA_BA_0 / GPIO2[8]
uP_EMIFA_D15	E6	EMA_D_15 / GPIO3[7]
uP_EMIFA_D14	C7	EMA_D_14 / GPIO3[6]
uP_EMIFA_D13	B6	EMA_D_13 / GPIO3[5]
uP_EMIFA_D12	A6	EMA_D_12 / GPIO3[4]
uP_EMIFA_D11	D6	EMA_D_11 / GPIO3[3]
uP_EMIFA_D10	A7	EMA_D_10 / GPIO3[2]
uP_EMIFA_D9	D9	EMA_D_9 / GPIO3[1]
uP_EMIFA_D8	E10	EMA_D_8 / GPIO3[0]
uP_EMIFA_D7	D7	EMA_D_7 / GPIO4[15]
uP_EMIFA_D6	C6	EMA_D_6 / GPIO4[14]
uP_EMIFA_D5	E7	EMA_D_5 / GPIO4[13]
uP_EMIFA_D4	B5	EMA_D_4 / GPIO4[12]
uP_EMIFA_D3	E8	EMA_D_3 / GPIO4[11]
uP_EMIFA_D2	B8	EMA_D_2 / GPIO4[10]
uP_EMIFA_D1	A8	EMA_D_1 / GPIO4[9]
uP_EMIFA_D0	C9	EMA_D_0 / GPIO4[8]
	B7	EMA_CLK / GPIO2[7]
	D8	EMA_SDCKE / GPIO2[6]
2 uP_EMIFA_CSn5	B16	EMA_CSn_5 / GPIO3[12]
2 uP_EMIFA_CSn4	E9	EMA_CSn_4 / GPIO3[13]
2 uP_EMIFA_CSn3	A17	EMA_CSn_3 / GPIO3[14]
2 uP_EMIFA_CSn2	B17	EMA_CSn_2 / GPIO3[15]
2 uP_EMIFA_CSn0	A18	EMA_CSn_0 / GPIO2[0]
2 uP_EMIFA_WEn	B9	EMA_WEn / GPIO3[11]
2 uP_EMIFA_OEn	B15	EMA_OEn / GPIO3[10]
	D10	EMA_A_RnW / GPIO3[9]
	A16	EMA_RASn / GPIO2[5]
	A9	EMA_CASn / GPIO2[4]
	A5	EMA_WEN_DQM_1 / GPIO2[2]
	C8	EMA_WEN_DQM_0 / GPIO2[3]
	B19	EMA_WAIT_1 / GPIO2[1]
	B18	EMA_WAIT_0 / GPIO3[8]
2 uP_TDI	M16	TDI
2 uP_TDO	J18	TDO
2 uP_TMS	L16	TMS
2 uP_TCK	J15	TCK
2 uP_TRSTn	L17	TRSTn
	K16	EMU1
	J16	EMU0
2 uP_RTCK	K17	RTCK / GPIO8[0]
	J17	NMIn
	T17	RESETOUTn / UHPI_HASn / GPIO6[15]
	K14	RESETn
2 uP_OBSCLK	T18	OBSCLK0 / UHPI_HDS2n / GPIO6[14]

R21 4.7k 5% 1002996
R22 4.7k 5% 1002996
R169 4.7k 5% 1002996
R25 4.7k 5% 1002996
R26 4.7k 5% 1002996

2 uP_EMIFA_RnW
7 PMIC_PBOUT
2 USB1_PWR_EN
7 PMIC_PWR_ON
7 PMIC_INTn
2 uP_EMIFA_WAIT1
2 uP_EMIFA_WAIT0

R28 4.7k 5% 1002996
R29 4.7k 5% 1002996
R30 4.7k 5% 1002996
R112 4.7k 5% 1002996
R170 4.7k 5% 1002996

2 uP_EMU1
2 uP_EMU0
2 uP_NMIn
2,5,6 uP_RESETOUTn
2,7 uP_RESETn

R31 22 5% 1001374

C56 0.1uF 1002396np
DGND

	T5	EMB_A_13
	V4	EMB_A_12
	T4	EMB_A_11
	W4	EMB_A_10
	T6	EMB_A_09
	U4	EMB_A_08
	U6	EMB_A_07
	W5	EMB_A_06
	V5	EMB_A_05
	U5	EMB_A_04
	V6	EMB_A_03
	W6	EMB_A_02
	T7	EMB_A_01
	U7	EMB_A_00
	U8	EMB_BA_2
	T9	EMB_BA_1
	V8	EMB_BA_0
uP_DDR_D15	W10	EMB_D_15
uP_DDR_D14	U11	EMB_D_14
uP_DDR_D13	V10	EMB_D_13
uP_DDR_D12	U10	EMB_D_12
uP_DDR_D11	T12	EMB_D_11
uP_DDR_D10	T10	EMB_D_10
uP_DDR_D9	T11	EMB_D_09
uP_DDR_D8	T13	EMB_D_08
uP_DDR_D7	W11	EMB_D_07
uP_DDR_D6	W12	EMB_D_06
uP_DDR_D5	V12	EMB_D_05
uP_DDR_D4	V13	EMB_D_04
uP_DDR_D3	U13	EMB_D_03
uP_DDR_D2	V14	EMB_D_02
uP_DDR_D1	U14	EMB_D_01
uP_DDR_D0	U15	EMB_D_00
uP_DDR_CLKP	W8	EMB_CLKP
uP_DDR_CLKN	W7	EMB_CLKN
uP_DDR_CKE 4	V7	EMB_CKE
uP_DDR_CSn 4	V9	EMB_CSn
uP_DDR_WEn 4	T8	EMB_WEn
uP_DDR_RASn 4	W9	EMB_RASn
uP_DDR_CASn 4	U9	EMB_CASn
uP_DDR_DQS1	V11	EMB_WEN_DQS_1
uP_DDR_DQS0	T14	EMB_WEN_DQS_0
DDR_STRBEN	R11	EMB_STRBEN
DDR_STRBEN_DEL	R12	EMB_STRBEN_DEL
uP_DDR_DQM1	R10	EMB_DQM_1
uP_DDR_DQM0	W13	EMB_DQM_0
	K18	USB0_DRVVBUSn
	N19	USB0_VBUS
	M18	USB0_DM
	M19	USB0_DP
uP_USB0_ID 2	P16	USB0_ID
	P18	USB1_DM
	P19	USB1_DP
	J19	RTC_XI
	H19	RTC_XO
	L19	OSCIN
	K19	OSCOUT

TP1

uP_DDR_A13
uP_DDR_A12
uP_DDR_A11
uP_DDR_A10
uP_DDR_A9
uP_DDR_A8
uP_DDR_A7
uP_DDR_A6
uP_DDR_A5
uP_DDR_A4
uP_DDR_A3
uP_DDR_A2
uP_DDR_A1
uP_DDR_A0
uP_DDR_BA1
uP_DDR_BA0

uP_DDR_A[13:0] 4
uP_DDR_BA[1:0] 4
DDR_D[15..0] 4

R6 22
4 5 DDR_D15
3 6 DDR_D14
2 7 DDR_D13
1 8 DDR_D12
1002428

R7 22
4 5 DDR_D11
3 6 DDR_D10
2 7 DDR_D9
1 8 DDR_D8
1002428

R8 22
1 8 DDR_D7
2 7 DDR_D6
3 6 DDR_D5
4 5 DDR_D4
1002428

R9 22
1 8 DDR_D3
2 7 DDR_D2
3 6 DDR_D1
4 5 DDR_D0
1002428

1002628 R10 10 5% DDR_CLKP 4
1002628 R11 10 5% DDR_CLKN 4

1001374
R17 22 5% DDR_DQS1 4
R18 22 5% DDR_DQS0 4
1001374

R19 0 1001368

1001374
R20 22 5% DDR_DQM1 4
R27 22 5% DDR_DQM0 4
1001374

USB_VBUS
uP_USB0_DRVVBUS 2

uP_USB0_DM 2
uP_USB0_DP 2

R151 24.9 1% 1003756
R152 24.9 1% 1003756
uP_USB1_DM 2
uP_USB1_DP 2

R153 15K 5% 1012888np
R154 15K 5% 1012888np
DGND

C5 18pF 1002955
RTC_VSS
Y1 32.768KHz FSX327LF 1001333
C6 18pF 1002955
RTC_VSS

C7 33pF 1005482
OSC_VSS
Y2 24MHZ CS10-24.000MABJ-UT 1006395
C8 33pF 1005482
OSC_VSS

LAYOUT NOTE: TARGET 50 OHMS TO GND FOR DATA SIGNALS - BOTH SIDES OF THE IN-LINE RESISTORS. KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: ROUTE THIS PAIR OF SIGNALS PHYSICALLY CLOSE TO THE DATA BUS. TOTAL TRACE LENGTH OF STRBEN + STRBEN_DEL SHOULD BE SUM OF DDR CLOCK LENGTH + AVG(DQS0 + DQS1) LENGTH. KEEP BOTH SIGNALS CLOSE TO EACH OTHER. THERE IS NO IMPEDANCE REQUIREMENT FOR THESE SIGNALS.

LAYOUT NOTE: ROUTE CLOCK SIGNALS AS 100 OHM DIFFERENTIAL PAIR. MATCH TRACE LENGTHS. TARGET 50 OHMS TO GND FOR EACH SIGNAL. KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: TARGET 50 OHMS TO GND FOR EACH SIGNAL. KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: ROUTE DM,DP AS 90 OHM DIFFERENTIAL PAIR WITH MATCHED TRACE LENGTHS. TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL 4 TRACES. KEEP AWAY FROM OTHER SIGNALS.

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Title OMAP-L138/C6748/AM1808 SOM-M1		Project PwrMeas	
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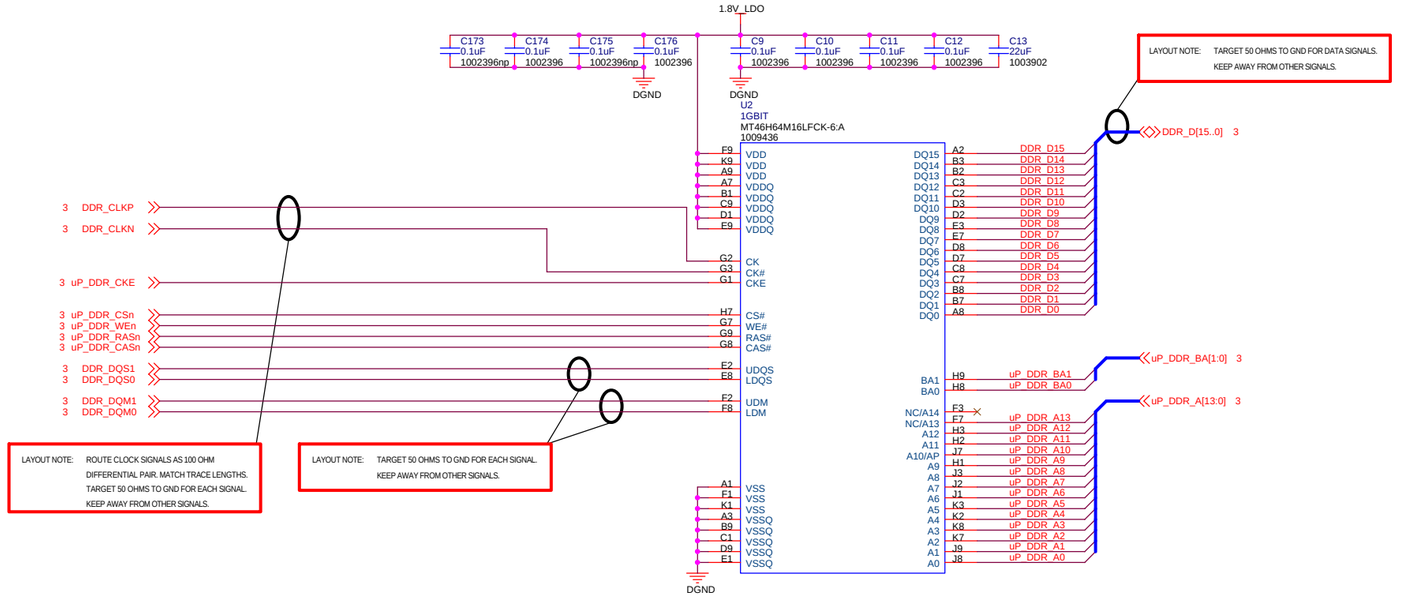
04 - DDR



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Title OMAP-L138/C6748/AM1808 SOM-M1		Project PwrMeas	
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05 - OMAP PERIPHERAL IF

U1B
OMAP-L138/C6748/AM1808
1012614

2 uP_VPIF_DIN[15..0]

uP_VPIF_DIN15 V18 — VPIF_DIN15_VSYNC / UHPI_HD7 / RPI_CH1_D7
uP_VPIF_DIN14 V19 — VPIF_DIN14_HSYNC / UHPI_HD6 / RPI_CH1_D6
uP_VPIF_DIN13 U19 — VPIF_DIN13_FIELD / UHPI_HD5 / RPI_CH1_D5
uP_VPIF_DIN12 T16 — VPIF_DIN12 / UHPI_HD4 / RPI_CH1_D4
uP_VPIF_DIN11 R18 — VPIF_DIN11 / UHPI_HD3 / RPI_CH1_D3
uP_VPIF_DIN10 R19 — VPIF_DIN10 / UHPI_HD2 / RPI_CH1_D2
uP_VPIF_DIN9 R15 — VPIF_DIN9 / UHPI_HD1 / RPI_CH1_D1
uP_VPIF_DIN8 P17 — VPIF_DIN8 / UHPI_HD0 / RPI_CH1_D0 / GPIO6[5]
uP_VPIF_DIN7 U18 — VPIF_DIN7 / UHPI_HD15 / RPI_CH1_D15 / EMAC_RMII_TXD[1]
uP_VPIF_DIN6 V16 — VPIF_DIN6 / UHPI_HD14 / RPI_CH1_D14 / EMAC_RMII_TXD[0]
uP_VPIF_DIN5 R14 — VPIF_DIN5 / UHPI_HD13 / RPI_CH1_D13 / EMAC_RMII_TXEN
uP_VPIF_DIN4 W16 — VPIF_DIN4 / UHPI_HD12 / RPI_CH1_D12 / EMAC_RMII_RXD[1]
uP_VPIF_DIN3 V17 — VPIF_DIN3 / UHPI_HD11 / RPI_CH1_D11 / EMAC_RMII_RXD[0]
uP_VPIF_DIN2 W17 — VPIF_DIN2 / UHPI_HD10 / RPI_CH1_D10 / EMAC_RMII_RXER
uP_VPIF_DIN1 W18 — VPIF_DIN1 / UHPI_HD9 / RPI_CH1_D9 / EMAC_RMII_MHZ_50_CLK
uP_VPIF_DIN0 W19 — VPIF_DIN0 / UHPI_HD8 / RPI_CH1_D8 / EMAC_RMII_CRS_DV

VPIF_DOUT15 / LCD_D_15 / RPI_XD7 / GPIO7[7] / BOOT7 — P4 uP_VPIF_DOUT15
VPIF_DOUT14 / LCD_D_14 / RPI_XD6 / GPIO7[6] / BOOT6 — R3 uP_VPIF_DOUT14
VPIF_DOUT13 / LCD_D_13 / RPI_XD5 / GPIO7[5] / BOOT5 — R2 uP_VPIF_DOUT13
VPIF_DOUT12 / LCD_D_12 / RPI_XD4 / GPIO7[4] / BOOT4 — R1 uP_VPIF_DOUT12
VPIF_DOUT11 / LCD_D_11 / RPI_XD3 / GPIO7[3] / BOOT3 — T3 uP_VPIF_DOUT11
VPIF_DOUT10 / LCD_D_10 / RPI_XD2 / GPIO7[2] / BOOT2 — T2 uP_VPIF_DOUT10
VPIF_DOUT9 / LCD_D_9 / RPI_XD1 / GPIO7[1] / BOOT1 — U3 uP_VPIF_DOUT9
VPIF_DOUT8 / LCD_D_8 / RPI_XD0 / GPIO7[0] / BOOT0 — U2 uP_VPIF_DOUT8
VPIF_DOUT7 / LCD_D_7 / RPI_XD15 / GPIO7[15] — U1 uP_VPIF_DOUT7
VPIF_DOUT6 / LCD_D_6 / RPI_XD14 / GPIO7[14] — V3 uP_VPIF_DOUT6
VPIF_DOUT5 / LCD_D_5 / RPI_XD13 / GPIO7[13] — V2 uP_VPIF_DOUT5
VPIF_DOUT4 / LCD_D_4 / RPI_XD12 / GPIO7[12] — V1 uP_VPIF_DOUT4
VPIF_DOUT3 / LCD_D_3 / RPI_XD11 / GPIO7[11] — W3 uP_VPIF_DOUT3
VPIF_DOUT2 / LCD_D_2 / RPI_XD10 / GPIO7[10] — W2 uP_VPIF_DOUT2
VPIF_DOUT1 / LCD_D_1 / RPI_XD9 / GPIO7[9] — W1 uP_VPIF_DOUT1
VPIF_DOUT0 / LCD_D_0 / RPI_XD8 / GPIO7[8] — H4 uP_VPIF_DOUT0

uP_VPIF_DOUT[15..0] 2

2 uP_VPIF_CLKIN3 — J3 — VPIF_CLKIN3 / MMCSD1_D1 / GPIO6[2]
2 uP_VPIF_CLKIN2 — H3 — VPIF_CLKIN2 / MMCSD1_D3 / GPIO6[4]
2 uP_VPIF_CLKIN1 — V15 — VPIF_CLKIN1 / UHPI_HDS1n / GPIO6[6]
2 uP_VPIF_CLKIN0 — W14 — VPIF_CLKIN0 / UHPI_HCSn / GPIO6[7] / RPI_2xTXCLK

MMCSD1_D5 / LCD_HSYNC / GPIO8[9] — G4 uP_LCD_HSYNC 2
MMCSD1_D4 / LCD_VSYNC / GPIO8[8] — F2 uP_LCD_VSYNC 2
MMCSD1_D6 / LCD_MCLK / GPIO8[10] — F1 uP_LCD_MCLK 2
MMCSD1_D7 / LCD_PCLK / GPIO8[11] — R5 uP_LCD_PCLK 2
LCD_AC_ENB_CSn / GPIO6[0] — uP_LCD_AC_ENB_CSn 2

1001374 R43 22 5% — 1001374 R44 22 5%

2,6 uP_SPI0_CLK — R45 22 1001374 — D19 — SPI0_CLK / EPWM0_A / GPIO1[8] / EMAC_MII_RXCLK
2,6 uP_SPI0_SOMI — C16 — SPI0_SOMI / EPWM0_SYNCI / GPIO8[6] / EMAC_MII_RXER
2,6 uP_SPI0_SIMO — C18 — SPI0_SIMO / EPWM0_SYNC / GPIO8[5] / EMAC_MII_CRS
2,6 uP_SPI0_ENAn — C17 — SPI0_ENAn / EPWM0_B / EMAC_MII_RXDV
2,6 uP_SPI0_SCSn5 — C19 — SPI0_SCSn_5 / UART0_RXD / GPIO8[4] / EMAC_MII_RXD[3]
2,6 uP_SPI0_SCSn4 — D18 — SPI0_SCSn_4 / UART0_TXD / GPIO8[3] / EMAC_MII_RXD[2]
2,6 uP_SPI0_SCSn3 — E17 — SPI0_SCSn_3 / UART0_CTSn / GPIO8[2] / EMAC_MII_RXD[1] / SATA_MP_SWITCH
2,6 uP_SPI0_SCSn2 — D16 — SPI0_SCSn_2 / UART0_RTSn / GPIO8[1] / EMAC_MII_RXD[0] / SATA_CP_DET
2,6 uP_SPI0_SCSn1 — E16 — SPI0_SCSn_1 / Timer64P0_OUT12 / GPIO1[7] / EMAC_MDIO_CLK / Timer64P0_IN12
2,6 uP_SPI0_SCSn0 — D17 — SPI0_SCSn_0 / Timer64P1_OUT12 / GPIO1[6] / EMAC_MDIO_D / Timer64P1_IN12

VPIF_CLKO3 / GPIO6[1] — K4 uP_VPIF_CLKO3 2
VPIF_CLKO2 / MMCSD1_D2 / GPIO6[3] — K3 uP_VPIF_CLKO2 2

1001374 R46 22
1001374 R47 22

uP_SPI1_CLK R50 22 1001374 — G19 — SPI1_CLK / GPIO2[13]
uP_SPI1_SOMI — H17 — SPI1_SOMI / GPIO2[11]
uP_SPI1_SIMO — G17 — SPI1_SIMO / GPIO2[12]
uP_SPI1_ENAn — H16 — SPI1_ENAn / GPIO2[12]
2,8 uP_SPI1_ENAn — G16 — SPI1_SCSn_7 / I2C0_SCL / Timer64P2_OUT12 / GPIO1[5]
2,7 uP_SPI1_SCSn7 — G18 — SPI1_SCSn_6 / I2C0_SDA / Timer64P3_OUT12 / GPIO1[4]
2,7 uP_SPI1_SCSn6 — F17 — SPI1_SCSn_5 / UART2_RXD / I2C1_SCL / GPIO1[3]
F16 — SPI1_SCSn_4 / UART2_TXD / I2C1_SDA / GPIO1[2]
2 uP_SPI1_SCSn3 — E18 — SPI1_SCSn_3 / UART1_RXD / SATA_LED / GPIO1[1]
2 uP_SPI1_SCSn2 — F19 — SPI1_SCSn_2 / UART1_TXD / SATA_CP_POD / GPIO1[0]
F18 — SPI1_SCSn_1 / EPWM1_A / GPIO2[15] / Timer64P2_IN12
uP_SPI1_SCSn0 — E19 — SPI1_SCSn_0 / EPWM1_B / GPIO2[14] / Timer64P3_IN12

1001374 R48 22

MMCSD1_D0 / RPI_CH0_CLK / GPIO8[15] — G2 uP_UPP_CH0_CLK 2
MMCSD1_CLK / RPI_CH0_START / GPIO8[14] — J4 uP_UPP_CH0_START 2
MMCSD1_CMD / RPI_CH0_ENABLE / GPIO8[13] — G3 uP_UPP_CH0_ENABLE 2
RPI_CH0_WAIT / GPIO8[12] — U17 uP_UPP_CH0_WAIT 2
UHPI_HCNTL0 / RPI_CH1_CLK / GPIO6[11] — W15 uP_UPP_CH1_CLK 2
UHPI_HCNTL1 / RPI_CH1_START / GPIO6[10] — U16 uP_UPP_CH1_START 2
UHPI_HHWIL / RPI_CH1_ENABLE / GPIO6[9] — T15 uP_UPP_CH1_ENABLE 2
UHPI_HRWn / RPI_CH1_WAIT / GPIO6[8] — R16 uP_UPP_CH1_WAIT 2
UHPI_HINTn / GPIO6[12] — R17 uP_UHPI_HINTn 2
UHPI_HRDY / GPIO6[13] — uP_UHPI_HRDY 2

1001374 R49 22

AXR6 / McBSP0_CLKR / GPIO1[14] / EMAC_MII_TXEN — C1 uP_McBSP0_CLKR 2,6
AXR5 / McBSP0_CLKX / GPIO1[13] / EMAC_MII_TXCLK — D3 uP_McBSP0_CLKX 2,6
AXR0 / ECAP1_APWM0 / GPIO8[7] / EMAC_MII_TXD[0] / McBSP0_CLKS — E3 uP_McBSP0_CLKS 2,6
AXR4 / McBSP0_FSR / GPIO1[12] / EMAC_MII_COL — D1 uP_McBSP0_FSR 2,6
AXR3 / McBSP0_FSX / GPIO1[11] / EMAC_MII_TXD[3] — E3 uP_McBSP0_FSX 2,6
AXR2 / McBSP0_DR / GPIO1[10] / EMAC_MII_TXD[2] — E2 uP_McBSP0_DR 2,6
AXR1 / McBSP0_DX / GPIO1[9] / EMAC_MII_TXD[1] — E1 uP_McBSP0_DX 2,6

1001374 R53 22
1001374 R54 22
1001374 R55 22

AXR14 / McBSP1_CLKR / GPIO0[6] — B4 uP_McBSP1_CLKR 2
AXR13 / McBSP1_CLKX / GPIO0[5] — B3 uP_McBSP1_CLKX 2
AXR8 / McBSP1_CLKS / ECAP1_APWM1 / GPIO0[0] — E4 uP_McBSP1_CLKS 2
AXR12 / McBSP1_FSR / GPIO0[4] — C4 uP_McBSP1_FSR 2
AXR11 / McBSP1_FSX / GPIO0[3] — C5 uP_McBSP1_FSX 2
AXR10 / McBSP1_DR / GPIO0[2] — D4 uP_McBSP1_DR 2
AXR9 / McBSP1_DX / GPIO0[1] — C3 uP_McBSP1_DX 2

1001374 R56 22
1001374 R57 22
1001374 R58 22

RSVD (AMUTEIN) / RTC_ALARM / UART2_CTSn / GPIO0[8] / DEEPSLEEPn — F4
AMUTE / UART2_RTSn / GPIO0[9] — D5
AXR7 / EPWMN1_TZ[0] / GPIO1[15] — D2
AXR15 / EPWMN0_TZ[0] / ECAP2_APWM2 / GPIO0[7] — A4
AFSX / GPIO0[12] — B2
AFSR / GPIO0[13] — C2
AHCLKX / USB_REFCLKIN / UART1_CTSn / GPIO0[10] — A3
AHCLKR / UART1_RTSn / GPIO0[11] — A2
ACLKX / GPIO0[14] — B1
ACLKR / GPIO0[15] — A1

2 uP_UART2_CTSn — R59 22 1001374
2 uP_UART2_RTSn — R60 22 1001374
2 uP_EPWM1_TZ[0] — R61 22 1001374
2 uP_McASP_FSX — R62 22 1001374
2 uP_McASP_FSR
2 uP_UART1_CTSn
2 uP_UART1_RTSn
2 uP_McASP_CLKX
2 uP_McASP_CLKR

SATA_REFCLKN — N1
SATA_REFCLKP — N2
SATA_TXN — J2 — uP_SATA_TXN 2
SATA_TXP — J1 — uP_SATA_TXP 2
SATA_RXN — L2 — uP_SATA_RXN 2
SATA_RXP — L1 — uP_SATA_RXP 2
SATA_AMUX — M3 — uP_SATA_AMUX — TP3

SATA_REFCLKN
SATA_REFCLKP

BOOTSTRAPS: DEFAULT IS SPI1

uP_VPIF_DOUT15 — boot7 R121 4.7k 1002996
uP_VPIF_DOUT14 — boot6 R122 4.7k 1002996
uP_VPIF_DOUT13 — boot5 R123 4.7k 1002996
uP_VPIF_DOUT12 — boot4 R124 4.7k 1002996
uP_VPIF_DOUT11 — boot3 — R125 4.7k 1002996
uP_VPIF_DOUT10 — boot2 — R126 4.7k 1002996
uP_VPIF_DOUT9 — boot1 R127 4.7k 1002996
uP_VPIF_DOUT8 — boot0 R128 4.7k 1002996

3.3V_or_1.8V
DGND

BOOT DEVICE OPTIONS

BOOT DEVICE	BOOT BITS[4:1]
NOR EMIFA	0001
NAND-8 EMIFA	0111
SPI0 FLASH	0101
SPI1 FLASH(default)	0110
UART0	1011
UART2	1010
EMULATOR DEBUG	1111

3.3V_or_1.8V
R51 1.0K 1% 1006388
R52 1.0K 1% 1006388
R179 4.7k 5% 1002996
2 uP_SPI1_SCSn5
2 uP_SPI1_SCSn4
2 uP_SPI1_SCSn1
LCD_BACKLIGHT_PWR
2 uP_EPWM0_TZ[0]
R168 1.0K 1% 1006388
DGND

VOLTAGE TRANSLATION

3.3V_or_1.8V
C16 0.1uF 1002396 DGND
3.3V_or_1.8V
3.3V
C17 0.1uF 1002396 DGND
U4
SN74AVC4T245RGYR
1012581
1DIR 1OE VCCA VCCB 1A1 1A2 2DIR 2OE 2A1 2A2 GND GND GND 1B1 1B2 2B1 2B2
R155 4.7k 5% 1002996np
R64 4.7k 5% 1002996
R65 4.7k 5% 1002996
R66 4.7k 5% 1002996
uP_SPI1_SIMO
uP_SPI1_CLK
uP_SPI1_ENAn
R171 0 1001368np
2,3,6 BUFF_OEn
uP_SPI1_SCSn0
2,3,6 uP_RESETOUTn
R172 1.0K 1% 1006388
R69 1.0K 1% 1006388
DGND

64Mbit BOOT FLASH

3.3V
C18 0.1uF 1002396 DGND
U6
64Mbit
M25P64-VME6TG
1012961
DIO DO CLK CS VCC HOLD WP GND GND
R63 4.7k 5% 1002996
R133 4.7k 5% 1002996
R134 4.7k 5% 1002996
R135 4.7k 5% 1002996
R67 4.7k 5% 1002996
R136 4.7k 5% 1002996
FLASH_DIN
FLASH_DOUT
FLASH_CLK
FLASH_CSn
uP_RESETOUTn_3v3
DGND

FB3
BLM18KG700TN1D
1012775
3.3V
C166 0.1uF 1002396
C167 0.1uF 1002396
C168 0.1uF 1002396
C169 10uF 1005620
C170 0.1uF 1002396
C171 0.1uF 1002396
C172 10uF 1005620
DGND

3.3V_or_1.8V
U3
SN74LVC1G125DCKR
1004669
VCC OE Y A GND
C14 0.1uF 1002396
uP_SPI1_SOMI
DGND

3.3V
R147 4.7k 5% 1002996
R148 4.7k 5% 1002996
R149 4.7k 5% 1002996
U20
CDCM61001RHBT
1012876
PR1 PR0 OD2 OD1 OD0 OS1 OS0 VCC_PLL1 VCC_PLL2 VCC_VCO VCC_IN VCC_OUT OUTP OUTN XIN CE RST NC NC NC NC NC NC NC NC GND1 GND REG_CAP2 REG_CAP1 NC NC NC OSC_OUT
R150 4.7k 5% 1002996
R178 4.7k 5% 1002996
3.3V
TP12
uP_RESETOUTn_3v3
2,3,6 BUFF_OEn
Q3
N-CH
FDV301N (RoHS)
1004441
DGND
R143 4.7k 5% 1002996
R144 4.7k 5% 1002996
R145 4.7k 5% 1002996
R146 4.7k 5% 1002996np
DGND
C163 10pF 1001330np
C164 10uF 1005620
C165 10uF 1005620
Y5
25.0000MHz
ECS-250-20-33-A-E-L-TR
1008355
DGND
DGND
TP13

100M_CLKP — C25 0.01uF 1001329 — R68 100 1% 1006383np — SATA_REFCLKP
100M_CLKN — C26 0.01uF 1001329 — SATA_REFCLKN

LAYOUT NOTE: KEEP IN-LINE CAPS CLOSE TO U20

LAYOUT NOTE: KEEP RESISTOR CLOSE TO PROCESSOR

LAYOUT NOTE: ROUTE "P" AND "N" PAIRS AS 100 OHM DIFFERENTIAL PAIRS WITH MATCHED TRACE LENGTHS.
TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL TRACES.
KEEP AWAY FROM OTHER SIGNALS.

OSCILLATOR SETTINGS:

INPUT CRYSTAL: 25MHZ
PRESCALER DIVIDER: 3
FEEDBACK DIVIDER: 24
OUTPUT DIVIDER: 6
OUTPUT FREQUENCY: 100MHZ
OUTPUT TYPE: LVDS

LVDS 100MHZ CLOCK GENERATOR

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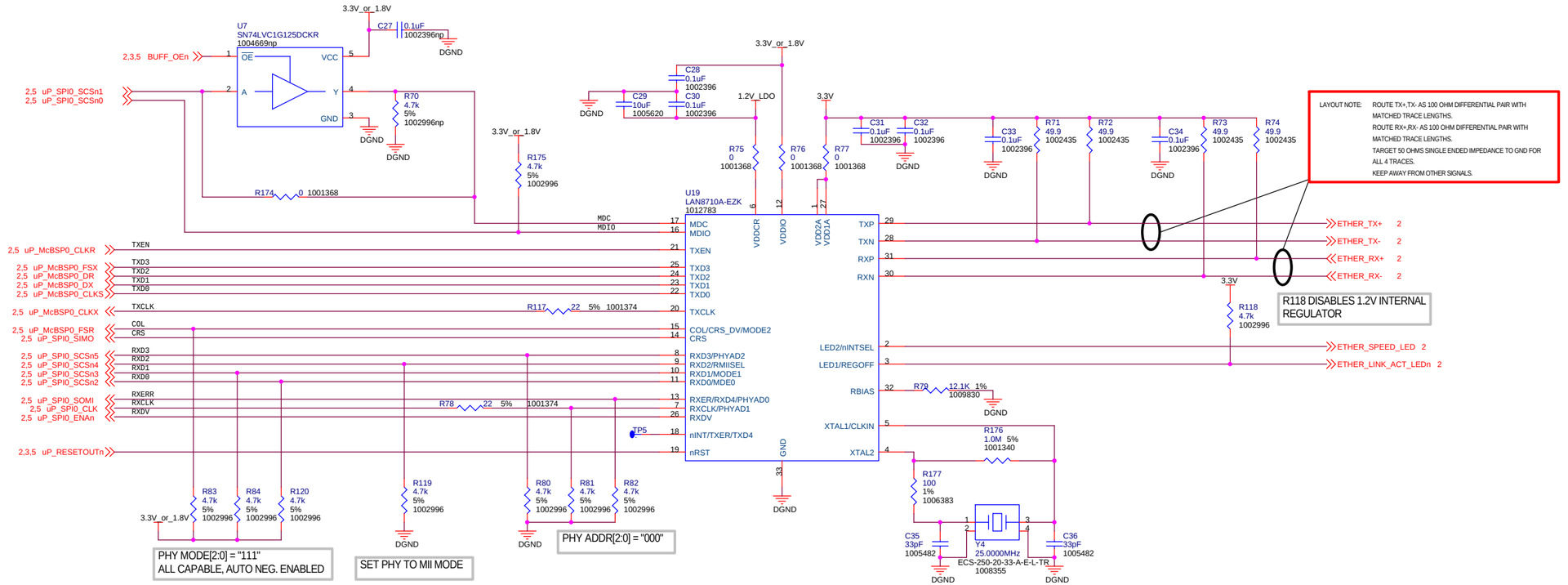
06 - ETHERNET PHY



PHY MODE CONFIGURATION TABLE

MODE[2:0]	MODE DEFINITION
000	10BASE-T HALF DUPLEX. AUTO-NEGOTIATION DISABLED.
001	10BASE-T FULL DUPLEX. AUTO-NEGOTIATION DISABLED.
010	100BASE-TX HALF DUPLEX. AUTO-NEGOTIATION DISABLED. CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
011	100BASE-TX FULL DUPLEX. AUTO-NEGOTIATION DISABLED.CRS IS ACTIVE DURING RECEIVE.
100	100BASE-TX HALF DUPLEX IS ADVERTISED. AUTONEGOTIATION ENABLED.CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
101	REPEATER MODE. AUTO-NEGOTIATION ENABLED.100BASE-TX HALF DUPLEX IS ADVERTISED.CRS IS ACTIVE DURING RECEIVE.
110	POWER DOWN MODE.
111	ALL CAPABLE. AUTO-NEGOTIATION ENABLED.

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07 - PMIC

Applying power to 5V_IN will cause SOM to power up immediately.

For startup without MAIN_BATT_IN connected, 5V_IN range is:
3.6V < 5V_IN < 5.8V
For startup with MAIN_BATT_IN connected, 5V_IN range is:
4.3V < 5V_IN < 5.8V

At runtime, 5V_IN range is:
UVLO < 5V_IN < 5.8V

UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)

Applying power to MAIN_BATT_IN will NOT cause SOM to power up immediately.
SOM will power up when power is supplied to MAIN_BATT_IN, and then PMIC_PB_IN is pulsed low.
PMIC_PB_IN must be pulsed low AFTER power is applied to MAIN_BATT_IN.

For startup, MAIN_BATT_IN range is:
3.6V < MAIN_BATT_IN < 4.2V

At runtime, MAIN_BATT_IN range is:
UVLO < MAIN_BATT_IN < 4.2V

UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)

5V POWER MEASURE
I2C ADDR: 1000000

LAYOUT NOTE: ROUTE THESE AS YOU WOULD A DIFFERENTIAL PAIR. TRY TO KEEP EACH PAIR AWAY FROM OTHER SIGNALS. THERE IS NO IMPEDANCE REQUIREMENT FOR THESE SIGNALS.

SET MAX CHARGE CURRENT TO 0.99A

DEFAULT: 3.3V IO VOLTAGE

PMIC I2C ADDR: 100 1000

LAYOUT NOTE: ROUTE THESE AS YOU WOULD A DIFFERENTIAL PAIR. TRY TO KEEP EACH PAIR AWAY FROM OTHER SIGNALS. THERE IS NO IMPEDANCE REQUIREMENT FOR THESE SIGNALS.

LAYOUT NOTE: CONNECT THE AGND PIN DIRECTLY TO THE CENTER GROUND PAD

RTC LDO

3.3V POWER MEASURE
I2C ADDR: 1000001

VIO POWER MEASURE
I2C ADDR: 1000010

1.2V POWER MEASURE
I2C ADDR: 1000011

1.2V LDO POWER MEASURE
I2C ADDR: 1000100

1.8V LDO POWER MEASURE
I2C ADDR: 1000101

1.2V RTC POWER MEASURE
I2C ADDR: 1000110

POWER MEASUREMENT ADDRESSING

POWER SUPPLY	I2C ADDRESS
5V MAIN	1000000
3.3V PMIC SWITCHER	1000001
1.8V/3.3V IO VOLTAGE PMIC SWITCHER	1000010
1.2V PMIC SWITCHER	1000011
1.2V PMIC LDO	1000100
1.8V PMIC LDO	1000101
1.2V RTC LDO	1000110

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08 - OMAP POWER

U1C
OMAP-L138/C6748/AM1808
1012614

1.8V_LDO
DVDD3318A
DVDD3318B
DVDD3318C

VDD18V: F14, G6, G10, G11, G12, J13, K5, L6, P13, R13, N6
VDDS [DDR_DVDD18]: N9, N10, P7, P8, P9, P10, R7, R8, R9
VDDSHV2 [DVDD3318_A]: F5, G5, H5
VDDSHV7 [DVDD3318_A]: F15, G14, G15, E14
VDDSHV [DVDD3318_B]: F6, F7, F8, F10, F11, F12, F13, G9, J14, K15
VDDSHV6 [DVDD3318_B]: J5, L4
VDDSHV3 [DVDD3318_C]: P5, P6, R4, K13, L13, M13, N13, P12
VDDSHV4 [DVDD3318_C]
VDDSHV5 [DVDD3318_C]

1.2V
1.2V_RTC
1.2V_LDO

VDD [CVDD]: N8, M9, M8, L12, K12, K6, J12, J6, H13, H12, H11, H10, H7, H6, G13, G8, G7, E15, L14
VDD2 [RTC_CVDD]: L14
VDDA12_PLL1: N15
VDDA12_PLL0: L15
VDDARNWA2: N7
VDDARNWA1: E5
VDDARNWA: H14
VPP [RSV]: T19
EMB_VREF: R6
EMB_PADREFP: U12
VDD3 [SATA_Vdd]: N4
SATA_VDDA: P2
SATA_VDDD: P1, M2
SATA_VDDR: P3
SATA_REG: N3
VDD4 [CVDD for USBs]: M12
VDDA12_USB0: N17
VDDA18_USB0: N14
VDD18_USB1: P14
VDD33_USB1: P15
VDDA33_USB0: N18

C63 0.1uF 1002396 DGND

1.2V_PLL1
C186 0.01uF 1001329
C187 0.1uF 1002396
AGND_PLL1
FB4 BLM18KG700TN1D 1012775
FB5 BLM18KG700TN1D 1012775
1.2V_LDO
DGND

LAYOUT NOTE: KEEP THESE COMPONENTS CLOSE TO THE PROCESSOR

1.2V_PLL0
C155 0.01uF 1001329
C154 0.1uF 1002396
AGND_PLL0
FB1 BLM18KG700TN1D 1012775
FB2 BLM18KG700TN1D 1012775
1.2V_LDO
DGND

LAYOUT NOTE: KEEP THESE COMPONENTS CLOSE TO THE PROCESSOR

TP4
R107 49.9 0.5% 1002435
DGND
EMB_VREF

1.8V_LDO
3.3V
C66 0.22uF 1006399
C67 0.22uF 1006399
DGND

1.8V_LDO
C64 0.1uF 1002396
R106 1.0K 1% 1006388
C65 0.1uF 1002396
R108 1.0K 1% 1006388
DGND

LAYOUT NOTE: KEEP THESE COMPONENTS CLOSE TO THE PROCESSOR

RTC_VSS
OSCVSS
VSSA12_PLL1
VSSA12_PLL0
VSSA_USB0
VSSA33_USB0
SATA_VSS
VSS
RTC_VSS
AGND_PLL1
OSC_VSS
AGND_PLL0
DGND

3.3V_or_1.8V 3.3V
R156 470 1008783
PRODUCT ID
3.3V
R157 1% 150K 1010439
U21 PCA9306 1012504
3.3V_or_1.8V
VREF1 VREF2 EN SCL1 SCL2 SDA1 SDA2 GND
2,5 uP_SPI1_ENAn
2,5 uP_UART2_CTSn
PID_CLK
PID_SDA
U22 Misc2 1012503
NC VCC CLK NC SDA NC GND NC
3.3V
DGND

1.2V
C68 22uF 1003902
C69 0.1uF 1002396
C75 0.1uF 1002396
C77 0.1uF 1002396
C104 0.1uF 1002396
C106 0.1uF 1002396
C110 0.1uF 1002396
C111 0.1uF 1002396
DGND

1.8V_LDO
C180 10uF 1005620
C181 10uF 1005620
C80 10uF 1005620
C81 0.1uF 1002396
C83 0.1uF 1002396
C87 0.1uF 1002396
C88 0.1uF 1002396
C115 0.1uF 1002396
C116 0.1uF 1002396
C120 0.1uF 1002396
C122 0.1uF 1002396
C113 0.1uF 1002396
DGND

DVDD3318A
C124 10uF 1005620
C126 0.1uF 1002396
C128 0.1uF 1002396
C129 0.1uF 1002396
C130 0.1uF 1002396
DGND

DVDD3318B
C131 10uF 1005620
C135 0.1uF 1002396
C138 0.1uF 1002396
C142 0.1uF 1002396
DGND

DVDD3318C
C143 10uF 1005620
C146 0.1uF 1002396
C151 0.1uF 1002396
C152 0.1uF 1002396
C153 0.1uF 1002396
DGND

JUMPERS ALLOW REWORK FOR IO VOLATGES OTHER THAN 3.3V OR 1.8V

3.3V_or_1.8V
R109 0 1001368 DVDD3318A
R110 0 1001368 DVDD3318B
R111 0 1001368 DVDD3318C

1.2V_LDO
C92 10uF 1005620
C93 0.1uF 1002396
C94 0.1uF 1002396
C95 0.1uF 1002396
C97 0.1uF 1002396
C99 0.1uF 1002396
DGND

3.3V
C100 10uF 1005620
C101 0.1uF 1002396
C102 0.1uF 1002396
DGND

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09 - ECO LIST

Revision Control			
Part Number	Rev	Description of Change	Date
1014647	A	Changed U3.1 to connect to net FLASH_CSn Added C182-C185	11-16-2009
1015115	A	Swapped location on J2 of ETHER_LINK_ACT_LEDn and ETHER_SPEED_LED Changed BATT_HDQ to uP_EPWM1_TZ[0] Added uP_EPWM0_TZ[0] to J2.99; uP_SPI1_SCSn0 to J3.36 Added R167-R172, R174-R179, Q3, C186-C187, FB4-FB5 Changed to np: R153, R154, R155, R70, U7, C27, C163 Removed R160, R161, C179, U24 Changed U1.C8 to PMIC_INTn; changed U9.40 to PMIC_INTn Added OSC_VSS and RTC_VSS nets Created net uP_RESETOUTn_3v3 Changed R105 to 1.0 Ohms from 0.02 Ohms; Changed R90 to 0603 part instead of 0805 part Changed R114 and R115 to 4.7k Ohms Removed net PIDCLK. Connected uP_SPI1_ENAn to U21.3. C154 and C155 moved to other side of ferrites	03-05-2010
1015115	B	Changed to np: Q1, Q2, R99, R100 Changed to pop: R116 Deleted C178 Added U24, L4, C188-C190, R180-R184, Q4	04-15-2010
1015115	C	Changed to np: R58 Changed C1, C2, C3, C4, C25, C26 to 0.01uF capacitors	09-24-2010

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