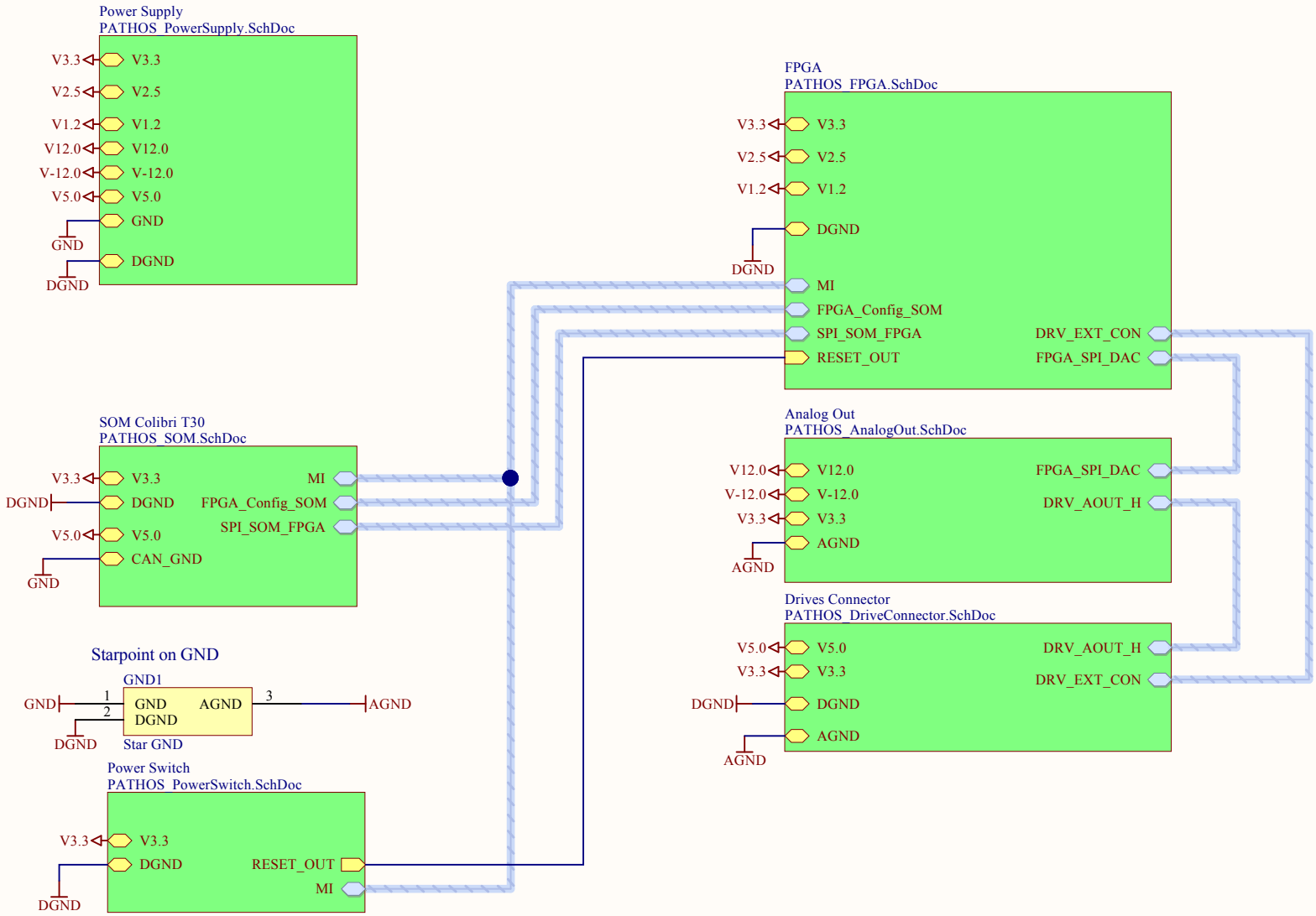

Title:	*Main Schematic*	
Description:		
Name: *A. Kalberer*		Checked: *
Size: *A4*	Number: *	Revision: *0.1*
Date: *28.09.2016*	Time: *16:33:19*	Sheet *1* of *2*
File: *D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_ControllerBoard*		

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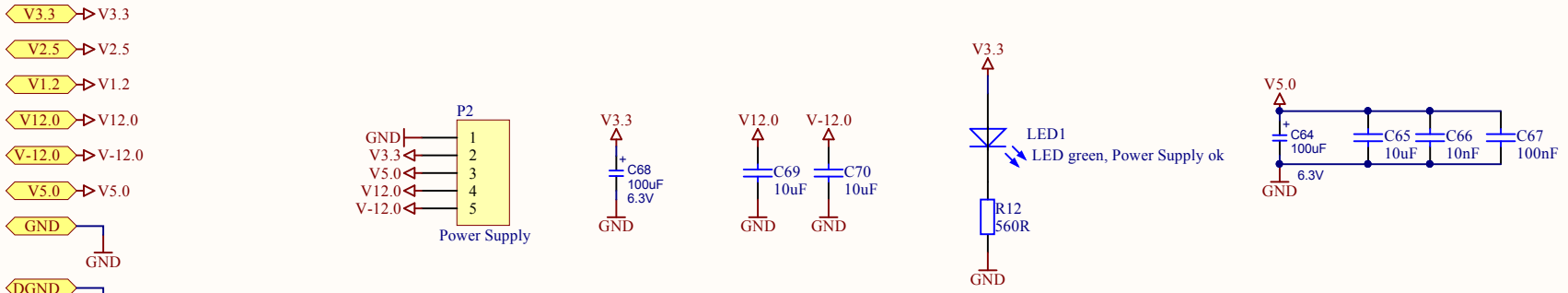
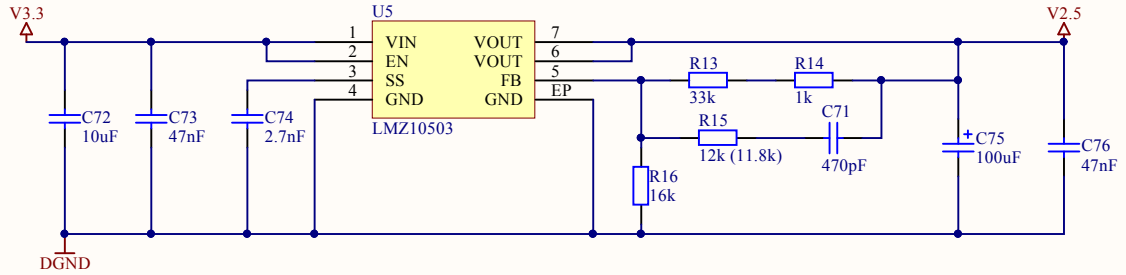
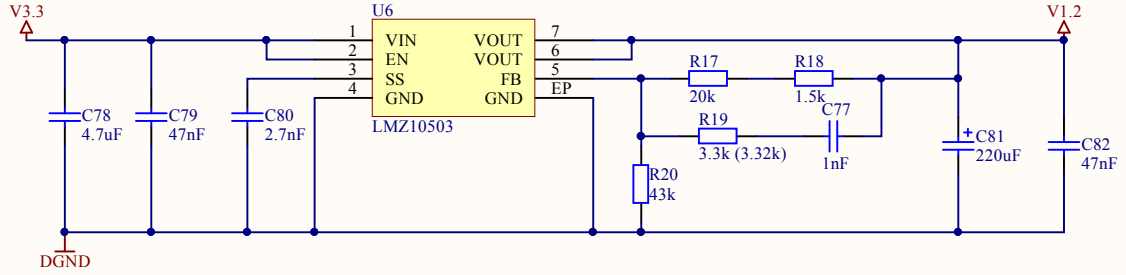


Output: 2.5V max. 3A



Output: 1.2V max. 3A



Title:	*Power Supply Main PCB*		
Description:	*Power Supply*		
Name:	*A. Kalberer*		Checked: *
Size:	*A4*	Number: *	Revision: *0.1*
Date:	*28.09.2016*	Time: *16:33:19*	Sheet *2* of *2*
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_PowerSupply.Sch*		

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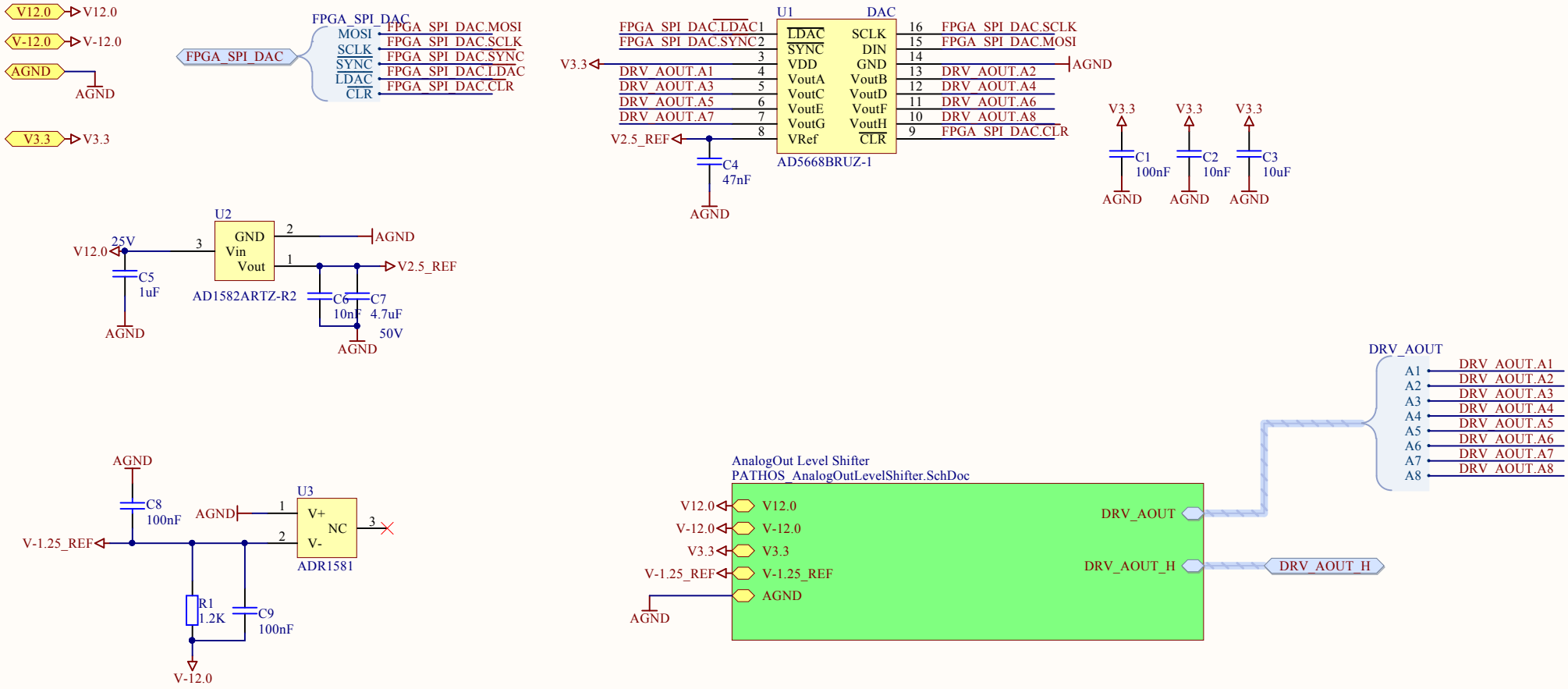

Title: *			
Description: *			
Name: *		Checked: *	
Size: A4	Number: *	Revision: *	
Date: 28.09.2016	Time: 16:33:19	Sheet * of *	
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_AnalogOut.SchD			

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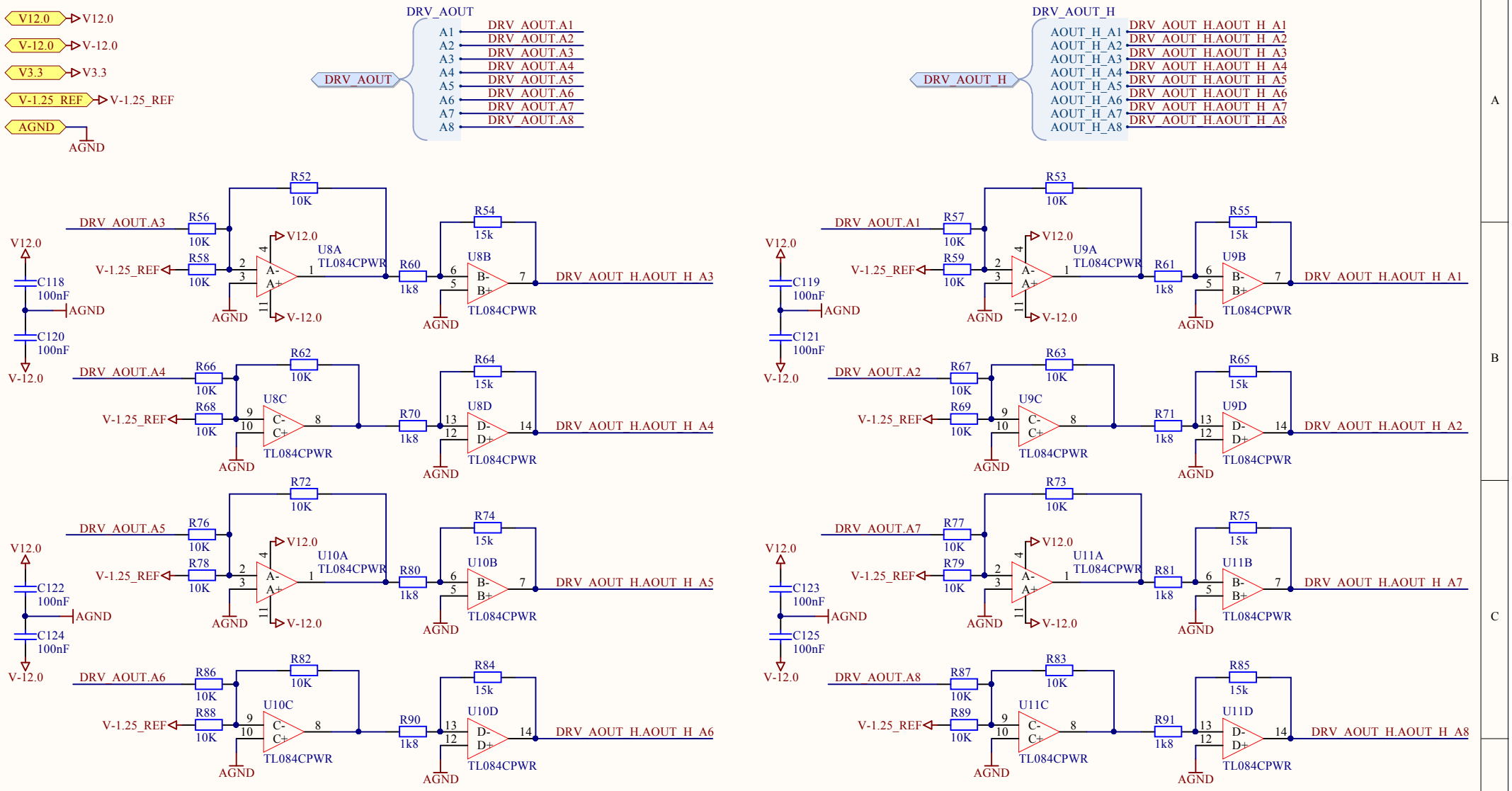

Title:	*Analog Out Level Shifter*
Description:	*+/-10V level shifter for analog out*
Name: *A. Kalberer*	Checked: *
Size: *A4*	Number: * Revision: *0.1*
Date: *28.09.2016*	Time: *16:33:19* Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_AnalogOutLevelS*

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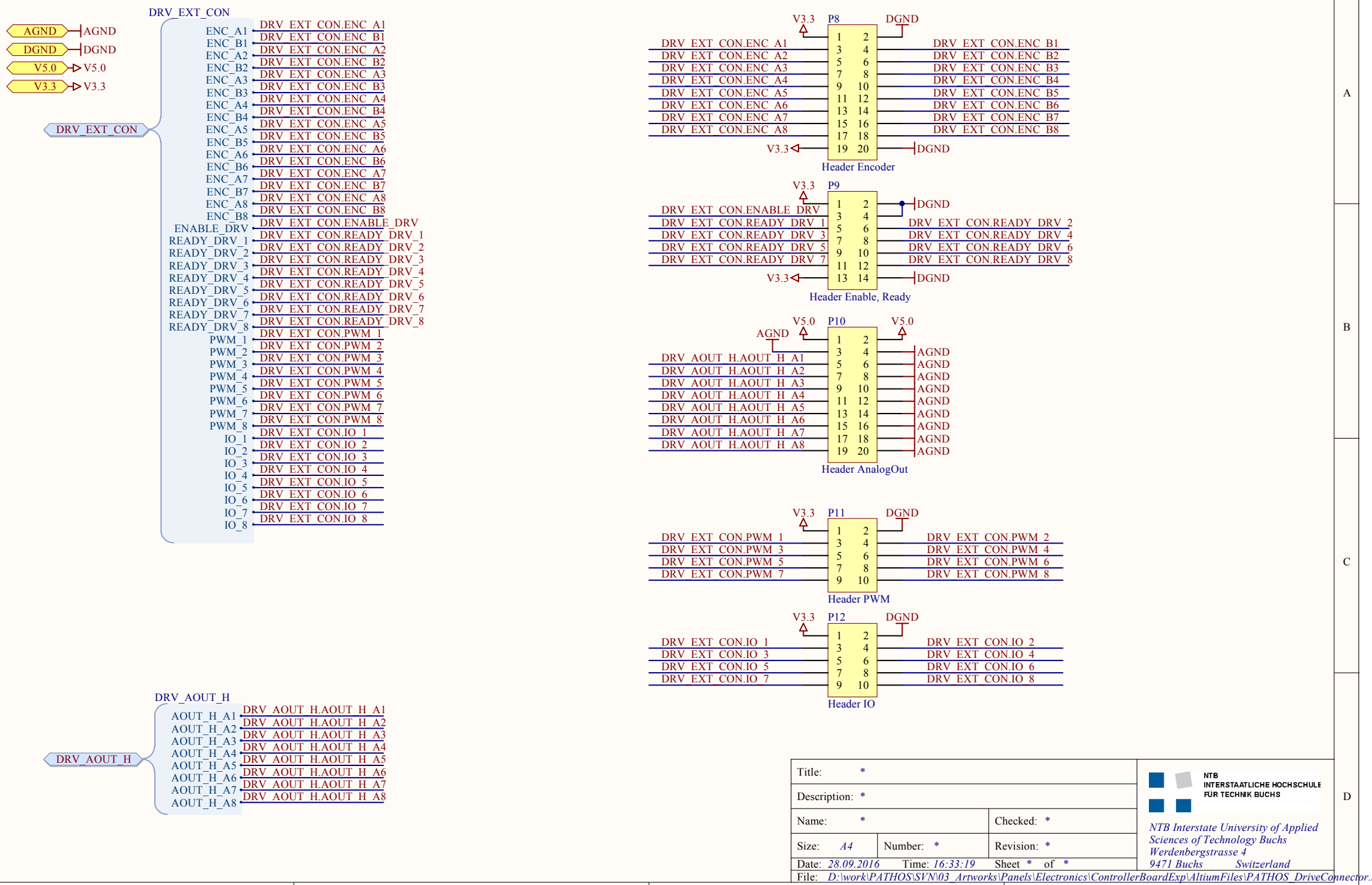
DRV_EXT_CON
AGND
DGND
V5.0
V3.3
ENC_A1 DRV_EXT_CON.ENC_A1
ENC_B1 DRV_EXT_CON.ENC_B1
ENC_A2 DRV_EXT_CON.ENC_A2
ENC_B2 DRV_EXT_CON.ENC_B2
ENC_A3 DRV_EXT_CON.ENC_A3
ENC_B3 DRV_EXT_CON.ENC_B3
ENC_A4 DRV_EXT_CON.ENC_A4
ENC_B4 DRV_EXT_CON.ENC_B4
ENC_A5 DRV_EXT_CON.ENC_A5
ENC_B5 DRV_EXT_CON.ENC_B5
ENC_A6 DRV_EXT_CON.ENC_A6
ENC_B6 DRV_EXT_CON.ENC_B6
ENC_A7 DRV_EXT_CON.ENC_A7
ENC_B7 DRV_EXT_CON.ENC_B7
ENC_A8 DRV_EXT_CON.ENC_A8
ENC_B8 DRV_EXT_CON.ENC_B8
ENABLE_DRV DRV_EXT_CON.ENABLE_DRV
READY_DRV_1 DRV_EXT_CON.READY_DRV_1
READY_DRV_2 DRV_EXT_CON.READY_DRV_2
READY_DRV_3 DRV_EXT_CON.READY_DRV_3
READY_DRV_4 DRV_EXT_CON.READY_DRV_4
READY_DRV_5 DRV_EXT_CON.READY_DRV_5
READY_DRV_6 DRV_EXT_CON.READY_DRV_6
READY_DRV_7 DRV_EXT_CON.READY_DRV_7
READY_DRV_8 DRV_EXT_CON.READY_DRV_8
PWM_1 DRV_EXT_CON.PWM_1
PWM_2 DRV_EXT_CON.PWM_2
PWM_3 DRV_EXT_CON.PWM_3
PWM_4 DRV_EXT_CON.PWM_4
PWM_5 DRV_EXT_CON.PWM_5
PWM_6 DRV_EXT_CON.PWM_6
PWM_7 DRV_EXT_CON.PWM_7
PWM_8 DRV_EXT_CON.PWM_8
IO_1 DRV_EXT_CON.IO_1
IO_2 DRV_EXT_CON.IO_2
IO_3 DRV_EXT_CON.IO_3
IO_4 DRV_EXT_CON.IO_4
IO_5 DRV_EXT_CON.IO_5
IO_6 DRV_EXT_CON.IO_6
IO_7 DRV_EXT_CON.IO_7
IO_8 DRV_EXT_CON.IO_8
DRV_AOUT_H
AOUT_H_A1 DRV_AOUT_H.AOUT_H_A1
AOUT_H_A2 DRV_AOUT_H.AOUT_H_A2
AOUT_H_A3 DRV_AOUT_H.AOUT_H_A3
AOUT_H_A4 DRV_AOUT_H.AOUT_H_A4
AOUT_H_A5 DRV_AOUT_H.AOUT_H_A5
AOUT_H_A6 DRV_AOUT_H.AOUT_H_A6
AOUT_H_A7 DRV_AOUT_H.AOUT_H_A7
AOUT_H_A8 DRV_AOUT_H.AOUT_H_A8
V3.3 P8 DGND
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
DRV_EXT_CON.ENC_A1 DRV_EXT_CON.ENC_B1
DRV_EXT_CON.ENC_A2 DRV_EXT_CON.ENC_B2
DRV_EXT_CON.ENC_A3 DRV_EXT_CON.ENC_B3
DRV_EXT_CON.ENC_A4 DRV_EXT_CON.ENC_B4
DRV_EXT_CON.ENC_A5 DRV_EXT_CON.ENC_B5
DRV_EXT_CON.ENC_A6 DRV_EXT_CON.ENC_B6
DRV_EXT_CON.ENC_A7 DRV_EXT_CON.ENC_B7
DRV_EXT_CON.ENC_A8 DRV_EXT_CON.ENC_B8
V3.3 DGND
Header Encoder
V3.3 P9 DGND
DRV_EXT_CON.ENABLE_DRV
DRV_EXT_CON.READY_DRV_1 DRV_EXT_CON.READY_DRV_2
DRV_EXT_CON.READY_DRV_3 DRV_EXT_CON.READY_DRV_4
DRV_EXT_CON.READY_DRV_5 DRV_EXT_CON.READY_DRV_6
DRV_EXT_CON.READY_DRV_7 DRV_EXT_CON.READY_DRV_8
V3.3 DGND
Header Enable, Ready
V5.0 P10 V5.0
AGND
DRV_AOUT_H.AOUT_H_A1 AGND
DRV_AOUT_H.AOUT_H_A2 AGND
DRV_AOUT_H.AOUT_H_A3 AGND
DRV_AOUT_H.AOUT_H_A4 AGND
DRV_AOUT_H.AOUT_H_A5 AGND
DRV_AOUT_H.AOUT_H_A6 AGND
DRV_AOUT_H.AOUT_H_A7 AGND
DRV_AOUT_H.AOUT_H_A8 AGND
Header AnalogOut
V3.3 P11 DGND
DRV_EXT_CON.PWM_1 DRV_EXT_CON.PWM_2
DRV_EXT_CON.PWM_3 DRV_EXT_CON.PWM_4
DRV_EXT_CON.PWM_5 DRV_EXT_CON.PWM_6
DRV_EXT_CON.PWM_7 DRV_EXT_CON.PWM_8
Header PWM
V3.3 P12 DGND
DRV_EXT_CON.IO_1 DRV_EXT_CON.IO_2
DRV_EXT_CON.IO_3 DRV_EXT_CON.IO_4
DRV_EXT_CON.IO_5 DRV_EXT_CON.IO_6
DRV_EXT_CON.IO_7 DRV_EXT_CON.IO_8
Header IO
Title: *
Description: *
Name: *
Checked: *
Size: A4
Number: *
Revision: *
Date: 28.09.2016 Time: 16:33:19 Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_DriveConnector.
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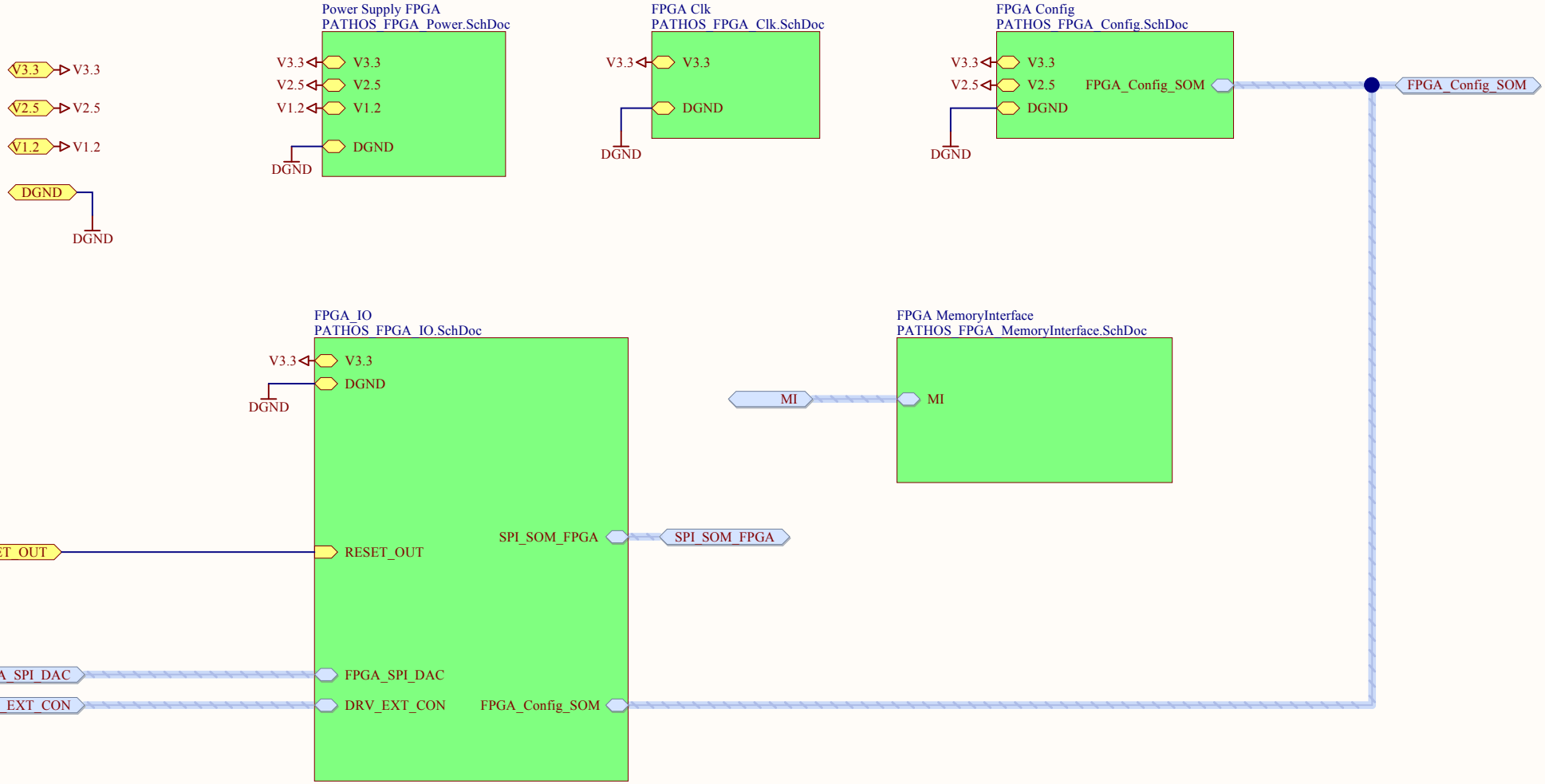

Title: *FPGA Overview*		
Description:		
Name: *A. Kalberer*		Checked: *
Size: *A4*	Number: *	Revision: *0.1*
Date: *28.09.2016* Time: *16:33:19*		Sheet * of *
File: *D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA.SchDoc*		

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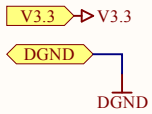

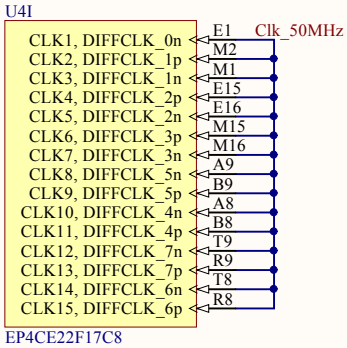

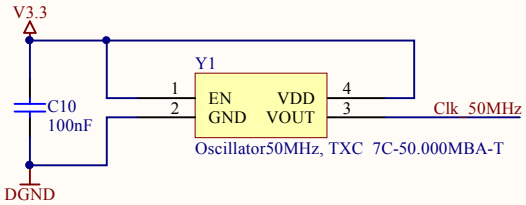

Title: *FPGA Clock*		
Description: *		
Name: *A. Kalberer*		Checked: *
Size: *A4*	Number: *	Revision: *
Date: *28.09.2016* Time: *16:33:19*		Sheet * of *
File: *D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA_Clk.SchD*		

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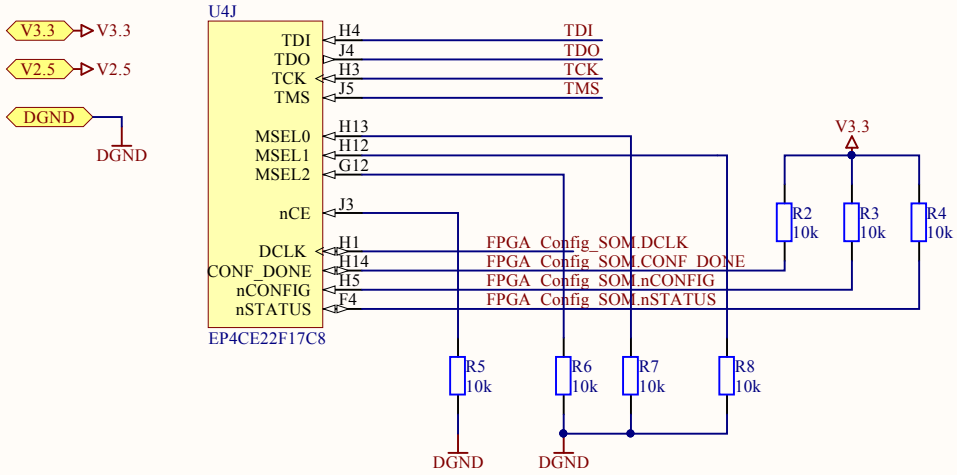
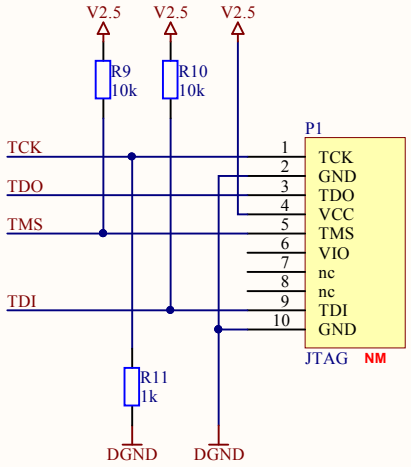


MSEL[0..2]: Config PS-Mode (0 0 0) see Cyclone IV Handbook page 173

JTAG



Title: *FPGA Config*		
Description:		
Name: *A. Kalberer*		Checked: *
Size: *A4*	Number: *	Revision: *
Date: *28.09.2016* Time: *16:33:19*		Sheet * of *
File: *D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA_Config.Sc*		

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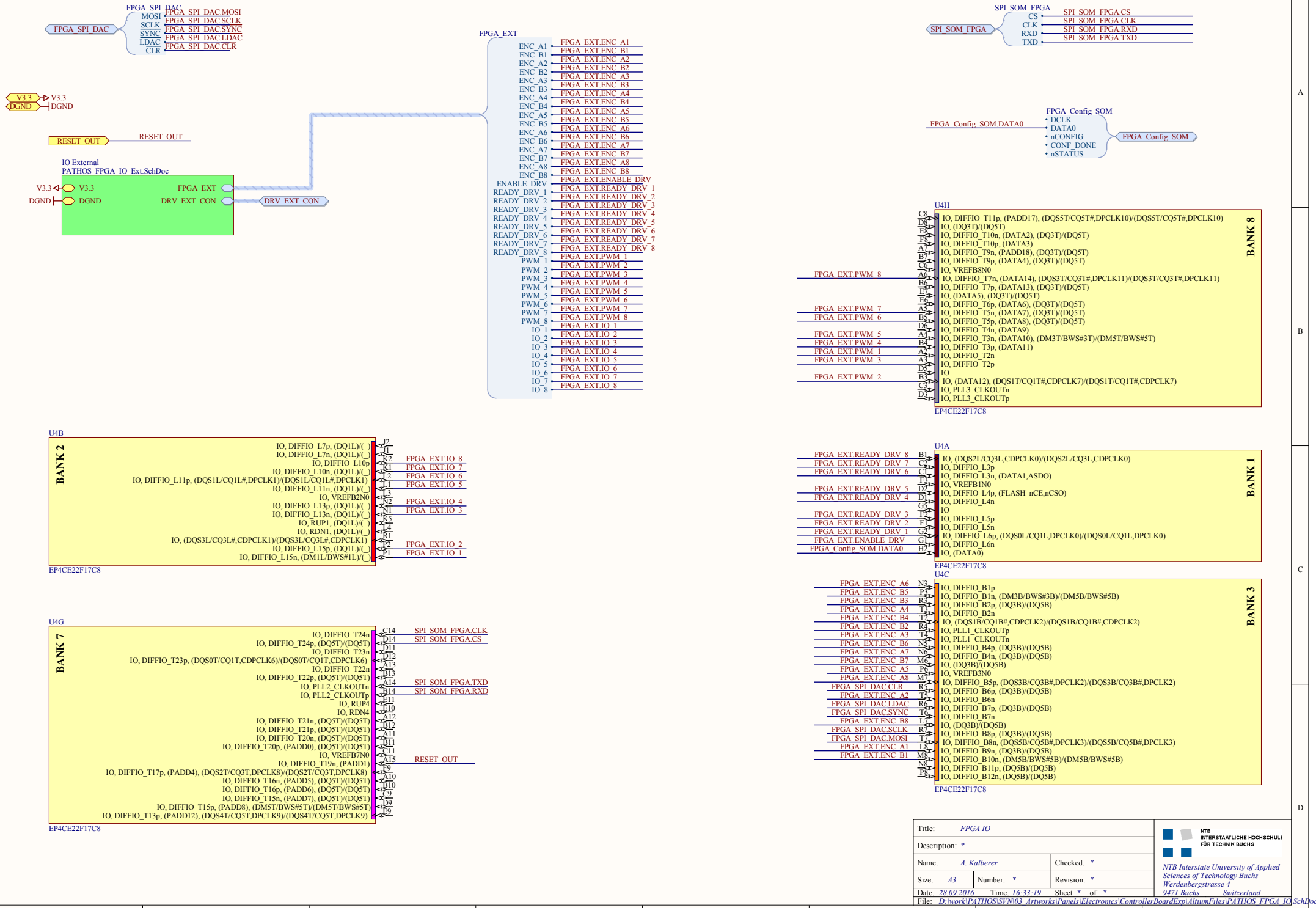
FPGA_SPI_DAC
FPGA_SPI_DAC.MOSI
FPGA_SPI_DAC.SCLK
FPGA_SPI_DAC.SYNC
FPGA_SPI_DAC.LDAC
FPGA_SPI_DAC.CLR
V3.3
DGND
RESET_OUT
IO External
PATHOS_FPGA_IO_Ext.SchDoc
FPGA_EXT
DRV_EXT_CON
SPI_SOM_FPGA
SPI_SOM_FPGA.CS
SPI_SOM_FPGA.CLK
SPI_SOM_FPGA.RXD
SPI_SOM_FPGA.TXD
FPGA_Config_SOM
FPGA_Config_SOM.DATA0
U4H
BANK 8
EP4CE22F17C8
U4B
BANK 2
U4A
BANK 1
U4C
BANK 3
U4G
BANK 7
Title: FPGA IO
Description: *
Name: A. Kalberer
Checked: *
Size: A3
Number: *
Revision: *
Date: 28.09.2016
Time: 16:33:19
Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA_IO.SchDoc
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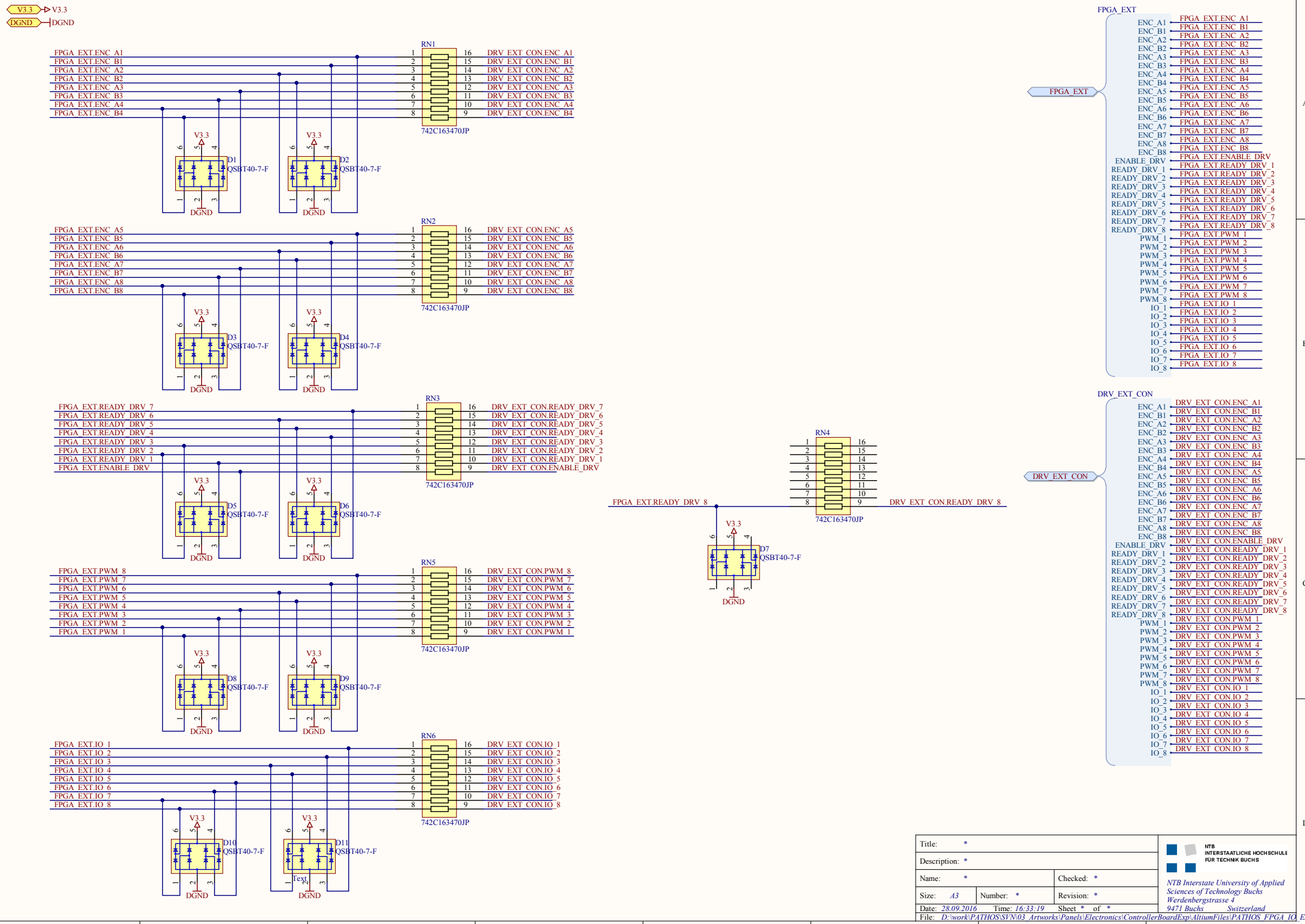
V3.3
DGND
RN1
FPGA_EXT.ENC_A1
FPGA_EXT.ENC_B1
FPGA_EXT.ENC_A2
FPGA_EXT.ENC_B2
FPGA_EXT.ENC_A3
FPGA_EXT.ENC_B3
FPGA_EXT.ENC_A4
FPGA_EXT.ENC_B4
DRV_EXT_CON.ENC_A1
DRV_EXT_CON.ENC_B1
DRV_EXT_CON.ENC_A2
DRV_EXT_CON.ENC_B2
DRV_EXT_CON.ENC_A3
DRV_EXT_CON.ENC_B3
DRV_EXT_CON.ENC_A4
DRV_EXT_CON.ENC_B4
742C163470JP
D1 QSBT40-7-F
D2 QSBT40-7-F
RN2
FPGA_EXT.ENC_A5
FPGA_EXT.ENC_B5
FPGA_EXT.ENC_A6
FPGA_EXT.ENC_B6
FPGA_EXT.ENC_A7
FPGA_EXT.ENC_B7
FPGA_EXT.ENC_A8
FPGA_EXT.ENC_B8
DRV_EXT_CON.ENC_A5
DRV_EXT_CON.ENC_B5
DRV_EXT_CON.ENC_A6
DRV_EXT_CON.ENC_B6
DRV_EXT_CON.ENC_A7
DRV_EXT_CON.ENC_B7
DRV_EXT_CON.ENC_A8
DRV_EXT_CON.ENC_B8
742C163470JP
D3 QSBT40-7-F
D4 QSBT40-7-F
RN3
FPGA_EXT.READY_DRV_7
FPGA_EXT.READY_DRV_6
FPGA_EXT.READY_DRV_5
FPGA_EXT.READY_DRV_4
FPGA_EXT.READY_DRV_3
FPGA_EXT.READY_DRV_2
FPGA_EXT.READY_DRV_1
FPGA_EXT.ENABLE_DRV
DRV_EXT_CON.READY_DRV_7
DRV_EXT_CON.READY_DRV_6
DRV_EXT_CON.READY_DRV_5
DRV_EXT_CON.READY_DRV_4
DRV_EXT_CON.READY_DRV_3
DRV_EXT_CON.READY_DRV_2
DRV_EXT_CON.READY_DRV_1
DRV_EXT_CON.ENABLE_DRV
742C163470JP
D5 QSBT40-7-F
D6 QSBT40-7-F
RN4
FPGA_EXT.READY_DRV_8
DRV_EXT_CON.READY_DRV_8
742C163470JP
D7 QSBT40-7-F
RN5
FPGA_EXT.PWM_8
FPGA_EXT.PWM_7
FPGA_EXT.PWM_6
FPGA_EXT.PWM_5
FPGA_EXT.PWM_4
FPGA_EXT.PWM_3
FPGA_EXT.PWM_2
FPGA_EXT.PWM_1
DRV_EXT_CON.PWM_8
DRV_EXT_CON.PWM_7
DRV_EXT_CON.PWM_6
DRV_EXT_CON.PWM_5
DRV_EXT_CON.PWM_4
DRV_EXT_CON.PWM_3
DRV_EXT_CON.PWM_2
DRV_EXT_CON.PWM_1
742C163470JP
D8 QSBT40-7-F
D9 QSBT40-7-F
RN6
FPGA_EXT.IO_1
FPGA_EXT.IO_2
FPGA_EXT.IO_3
FPGA_EXT.IO_4
FPGA_EXT.IO_5
FPGA_EXT.IO_6
FPGA_EXT.IO_7
FPGA_EXT.IO_8
DRV_EXT_CON.IO_1
DRV_EXT_CON.IO_2
DRV_EXT_CON.IO_3
DRV_EXT_CON.IO_4
DRV_EXT_CON.IO_5
DRV_EXT_CON.IO_6
DRV_EXT_CON.IO_7
DRV_EXT_CON.IO_8
742C163470JP
D10 QSBT40-7-F
D11 QSBT40-7-F
Text
FPGA_EXT
ENC_A1 FPGA_EXT.ENC_A1
ENC_B1 FPGA_EXT.ENC_B1
ENC_A2 FPGA_EXT.ENC_A2
ENC_B2 FPGA_EXT.ENC_B2
ENC_A3 FPGA_EXT.ENC_A3
ENC_B3 FPGA_EXT.ENC_B3
ENC_A4 FPGA_EXT.ENC_A4
ENC_B4 FPGA_EXT.ENC_B4
ENC_A5 FPGA_EXT.ENC_A5
ENC_B5 FPGA_EXT.ENC_B5
ENC_A6 FPGA_EXT.ENC_A6
ENC_B6 FPGA_EXT.ENC_B6
ENC_A7 FPGA_EXT.ENC_A7
ENC_B7 FPGA_EXT.ENC_B7
ENC_A8 FPGA_EXT.ENC_A8
ENC_B8 FPGA_EXT.ENC_B8
ENABLE_DRV FPGA_EXT.ENABLE_DRV
READY_DRV_1 FPGA_EXT.READY_DRV_1
READY_DRV_2 FPGA_EXT.READY_DRV_2
READY_DRV_3 FPGA_EXT.READY_DRV_3
READY_DRV_4 FPGA_EXT.READY_DRV_4
READY_DRV_5 FPGA_EXT.READY_DRV_5
READY_DRV_6 FPGA_EXT.READY_DRV_6
READY_DRV_7 FPGA_EXT.READY_DRV_7
READY_DRV_8 FPGA_EXT.READY_DRV_8
PWM_1 FPGA_EXT.PWM_1
PWM_2 FPGA_EXT.PWM_2
PWM_3 FPGA_EXT.PWM_3
PWM_4 FPGA_EXT.PWM_4
PWM_5 FPGA_EXT.PWM_5
PWM_6 FPGA_EXT.PWM_6
PWM_7 FPGA_EXT.PWM_7
PWM_8 FPGA_EXT.PWM_8
IO_1 FPGA_EXT.IO_1
IO_2 FPGA_EXT.IO_2
IO_3 FPGA_EXT.IO_3
IO_4 FPGA_EXT.IO_4
IO_5 FPGA_EXT.IO_5
IO_6 FPGA_EXT.IO_6
IO_7 FPGA_EXT.IO_7
IO_8 FPGA_EXT.IO_8
DRV_EXT_CON
ENC_A1 DRV_EXT_CON.ENC_A1
ENC_B1 DRV_EXT_CON.ENC_B1
ENC_A2 DRV_EXT_CON.ENC_A2
ENC_B2 DRV_EXT_CON.ENC_B2
ENC_A3 DRV_EXT_CON.ENC_A3
ENC_B3 DRV_EXT_CON.ENC_B3
ENC_A4 DRV_EXT_CON.ENC_A4
ENC_B4 DRV_EXT_CON.ENC_B4
ENC_A5 DRV_EXT_CON.ENC_A5
ENC_B5 DRV_EXT_CON.ENC_B5
ENC_A6 DRV_EXT_CON.ENC_A6
ENC_B6 DRV_EXT_CON.ENC_B6
ENC_A7 DRV_EXT_CON.ENC_A7
ENC_B7 DRV_EXT_CON.ENC_B7
ENC_A8 DRV_EXT_CON.ENC_A8
ENC_B8 DRV_EXT_CON.ENC_B8
ENABLE_DRV DRV_EXT_CON.ENABLE_DRV
READY_DRV_1 DRV_EXT_CON.READY_DRV_1
READY_DRV_2 DRV_EXT_CON.READY_DRV_2
READY_DRV_3 DRV_EXT_CON.READY_DRV_3
READY_DRV_4 DRV_EXT_CON.READY_DRV_4
READY_DRV_5 DRV_EXT_CON.READY_DRV_5
READY_DRV_6 DRV_EXT_CON.READY_DRV_6
READY_DRV_7 DRV_EXT_CON.READY_DRV_7
READY_DRV_8 DRV_EXT_CON.READY_DRV_8
PWM_1 DRV_EXT_CON.PWM_1
PWM_2 DRV_EXT_CON.PWM_2
PWM_3 DRV_EXT_CON.PWM_3
PWM_4 DRV_EXT_CON.PWM_4
PWM_5 DRV_EXT_CON.PWM_5
PWM_6 DRV_EXT_CON.PWM_6
PWM_7 DRV_EXT_CON.PWM_7
PWM_8 DRV_EXT_CON.PWM_8
IO_1 DRV_EXT_CON.IO_1
IO_2 DRV_EXT_CON.IO_2
IO_3 DRV_EXT_CON.IO_3
IO_4 DRV_EXT_CON.IO_4
IO_5 DRV_EXT_CON.IO_5
IO_6 DRV_EXT_CON.IO_6
IO_7 DRV_EXT_CON.IO_7
IO_8 DRV_EXT_CON.IO_8
Title: *
Description: *
Name: *
Checked: *
Size: A3
Number: *
Revision: *
Date: 28.09.2016
Time: 16:33:19
Sheet * of *
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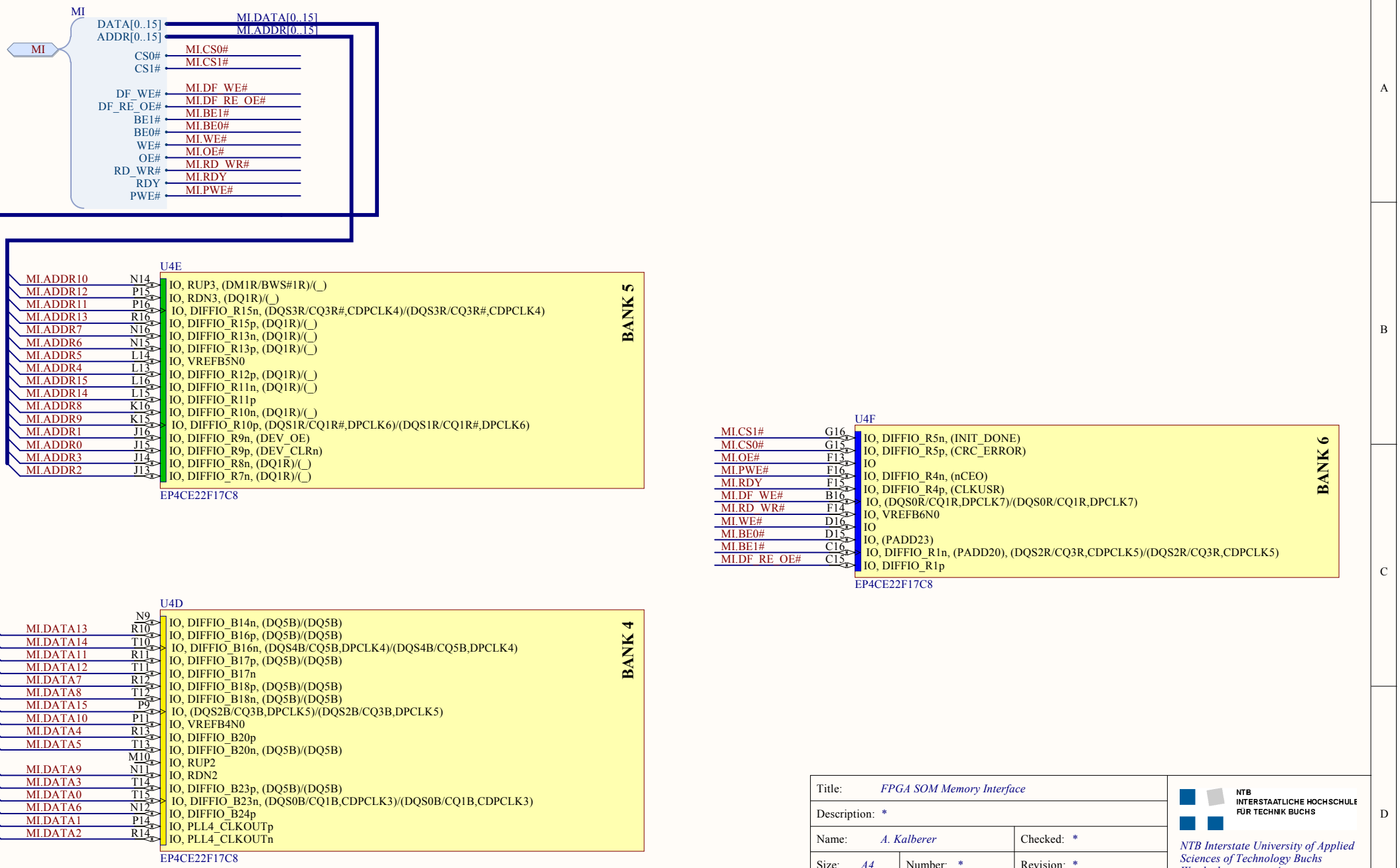
MI
DATA[0..15]
ADDR[0..15]
MI
CS0#
CS1#
DF_WE#
DF_RE_OE#
BE1#
BE0#
WE#
OE#
RD_WR#
RDY
PWE#
MI.DATA[0..15]
MI.ADDR[0..15]
MI.CS0#
MI.CS1#
MI.DF_WE#
MI.DF_RE_OE#
MI.BE1#
MI.BE0#
MI.WE#
MI.OE#
MI.RD_WR#
MI.RDY
MI.PWE#
U4E
MI.ADDR10 N14
MI.ADDR12 P15
MI.ADDR11 P16
MI.ADDR13 R16
MI.ADDR7 N16
MI.ADDR6 N15
MI.ADDR5 L14
MI.ADDR4 L13
MI.ADDR15 L16
MI.ADDR14 L15
MI.ADDR8 K16
MI.ADDR9 K15
MI.ADDR1 J16
MI.ADDR0 J15
MI.ADDR3 J14
MI.ADDR2 J13
IO, RUP3, (DM1R/BWS#1R)/(_)
IO, RDN3, (DQ1R)/(_)
IO, DIFFIO_R15n, (DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)
IO, DIFFIO_R15p, (DQ1R)/(_)
IO, DIFFIO_R13n, (DQ1R)/(_)
IO, DIFFIO_R13p, (DQ1R)/(_)
IO, VREFB5N0
IO, DIFFIO_R12p, (DQ1R)/(_)
IO, DIFFIO_R11n, (DQ1R)/(_)
IO, DIFFIO_R11p
IO, DIFFIO_R10n, (DQ1R)/(_)
IO, DIFFIO_R10p, (DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)
IO, DIFFIO_R9n, (DEV_OE)
IO, DIFFIO_R9p, (DEV_CLRn)
IO, DIFFIO_R8n, (DQ1R)/(_)
IO, DIFFIO_R7n, (DQ1R)/(_)
BANK 5
EP4CE22F17C8
U4F
MI.CS1# G16
MI.CS0# G15
MI.OE# F13
MI.PWE# F16
MI.RDY F15
MI.DF_WE# B16
MI.RD_WR# F14
MI.WE# D16
MI.BE0# D15
MI.BE1# C16
MI.DF_RE_OE# C15
IO, DIFFIO_R5n, (INIT_DONE)
IO, DIFFIO_R5p, (CRC_ERROR)
IO
IO, DIFFIO_R4n, (nCEO)
IO, DIFFIO_R4p, (CLKUSR)
IO, (DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)
IO, VREFB6N0
IO
IO, (PADD23)
IO, DIFFIO_R1n, (PADD20), (DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)
IO, DIFFIO_R1p
BANK 6
EP4CE22F17C8
U4D
N9
MI.DATA13 R10
MI.DATA14 T10
MI.DATA11 R11
MI.DATA12 T11
MI.DATA7 R12
MI.DATA8 T12
MI.DATA15 P9
MI.DATA10 P11
MI.DATA4 R13
MI.DATA5 T13
M10
MI.DATA9 N11
MI.DATA3 T14
MI.DATA0 T15
MI.DATA6 N12
MI.DATA1 P14
MI.DATA2 R14
IO, DIFFIO_B14n, (DQ5B)/(DQ5B)
IO, DIFFIO_B16p, (DQ5B)/(DQ5B)
IO, DIFFIO_B16n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)
IO, DIFFIO_B17p, (DQ5B)/(DQ5B)
IO, DIFFIO_B17n
IO, DIFFIO_B18p, (DQ5B)/(DQ5B)
IO, DIFFIO_B18n, (DQ5B)/(DQ5B)
IO, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)
IO, VREFB4N0
IO, DIFFIO_B20p
IO, DIFFIO_B20n, (DQ5B)/(DQ5B)
IO, RUP2
IO, RDN2
IO, DIFFIO_B23p, (DQ5B)/(DQ5B)
IO, DIFFIO_B23n, (DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)
IO, DIFFIO_B24p
IO, PLL4_CLKOUTp
IO, PLL4_CLKOUTn
BANK 4
EP4CE22F17C8
Title: FPGA SOM Memory Interface
Description: *
Name: A. Kalberer
Checked: *
Size: A4
Number: *
Revision: *
Date: 28.09.2016 Time: 16:33:19 Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA_MemoryI
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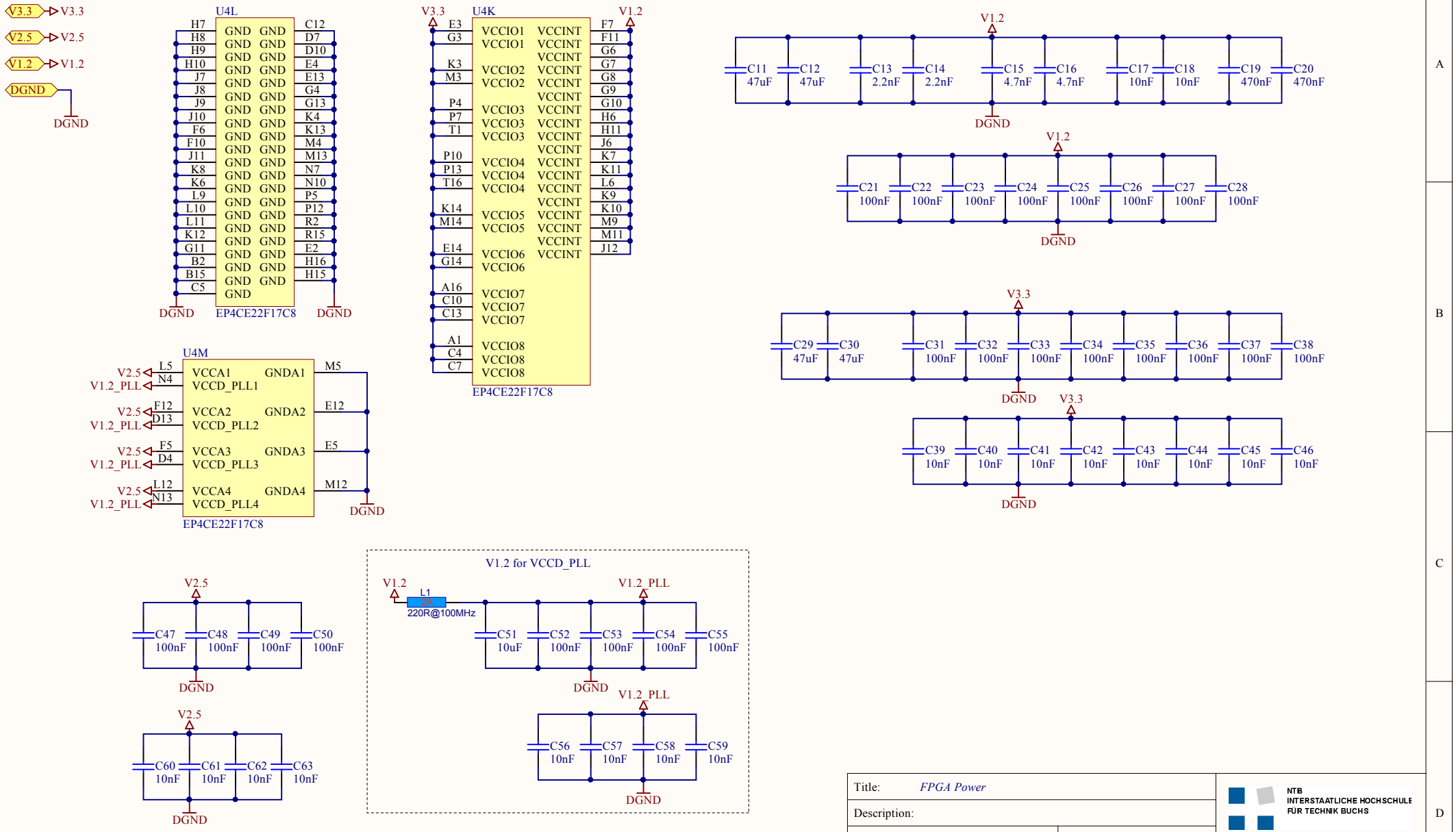

Title:	*FPGA Power*		
Description:			
Name:	*A. Kalberer*	Checked:	*
Size:	*A4*	Number: *	Revision: *
Date:	*28.09.2016*	Time: *16:33:19*	Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_FPGA_Power.Sc*		

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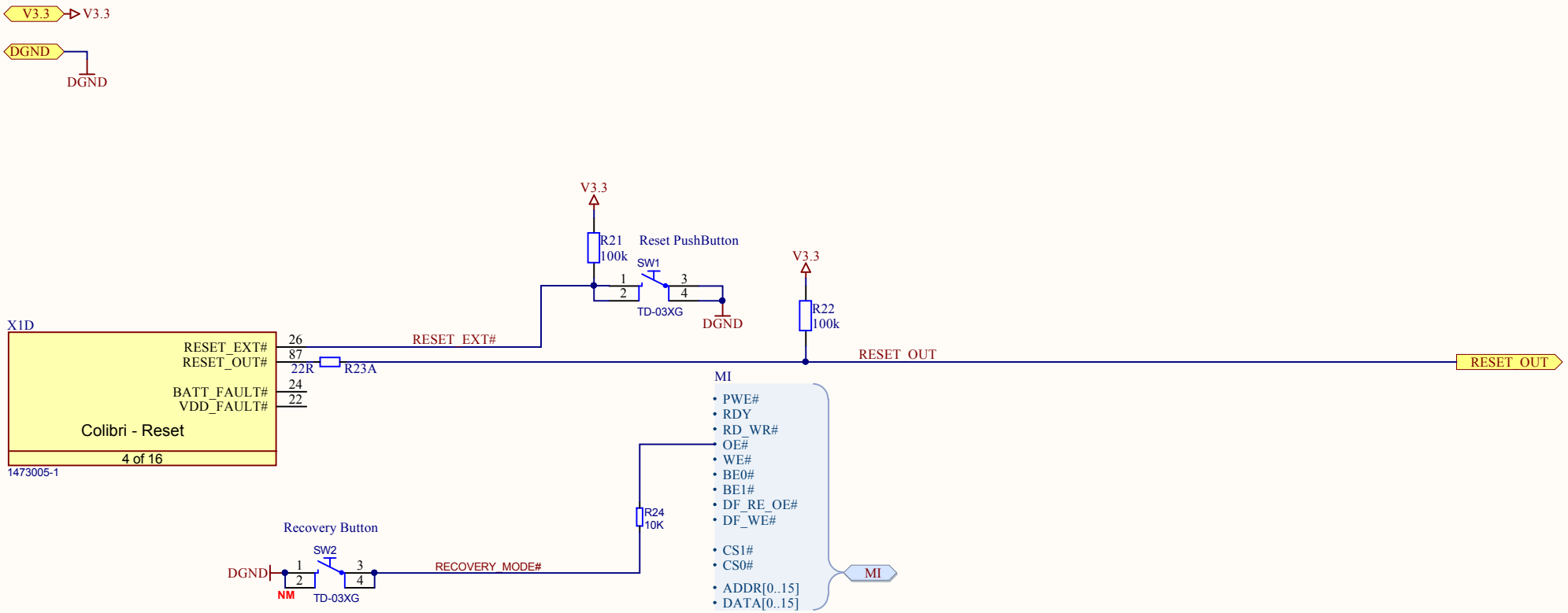

Title:	*Power Switch Schematic*		
Description:	*Power-, Reset-, Recovery-Circuit*		
Name:	*A. Kalberer*		Checked: *
Size:	*A4*	Number: *	Revision: *
Date:	*28.09.2016* Time: *16:33:20*		Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_PowerSwitch.Sch*		

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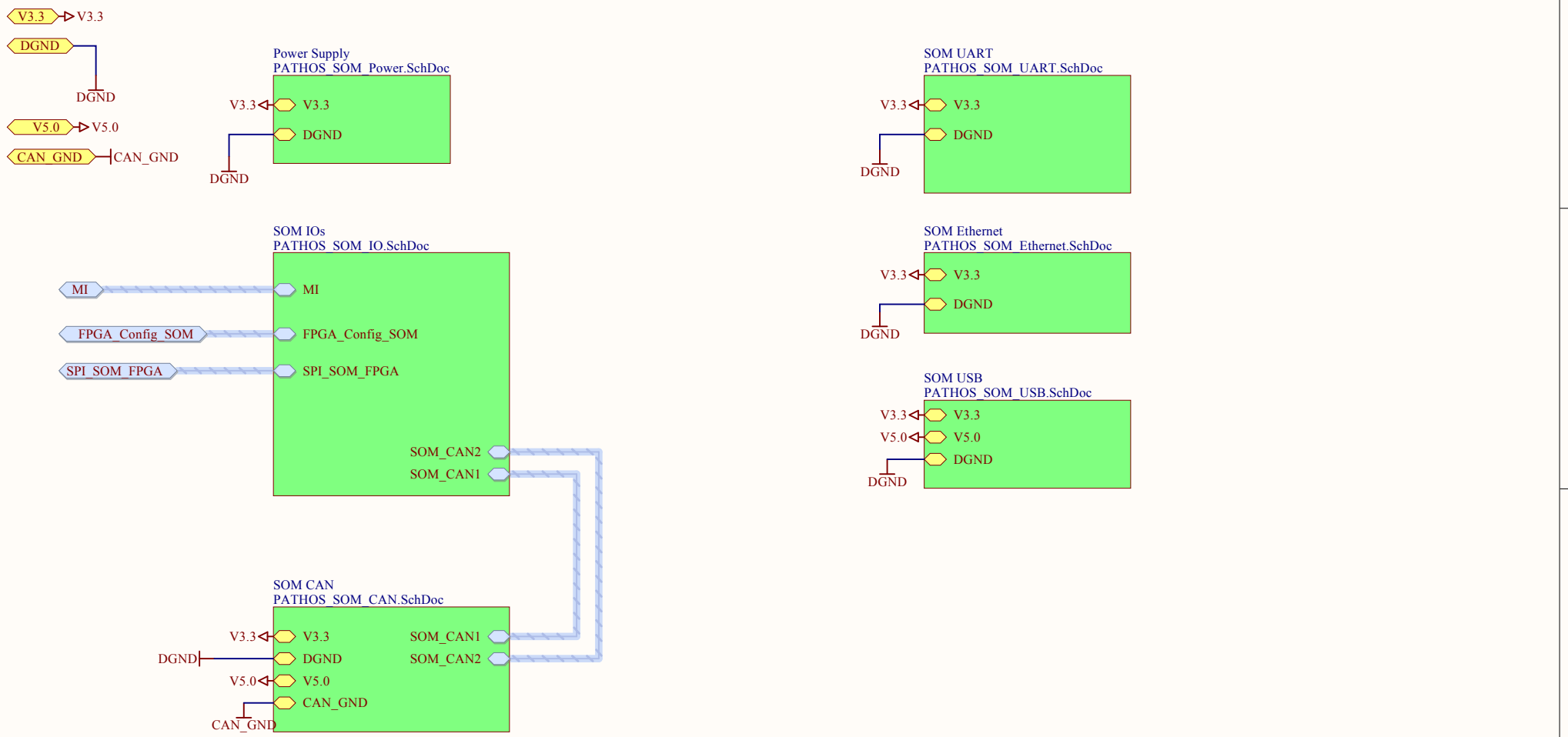

Title:	*SOM Main Schematic*		
Description:			
Name:	*A. Kalberer*		Checked: *
Size:	*A4*	Number: *	Revision: *
Date:	*28.09.2016*	Time: *16:33:20*	Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_SOM.SchDoc*		

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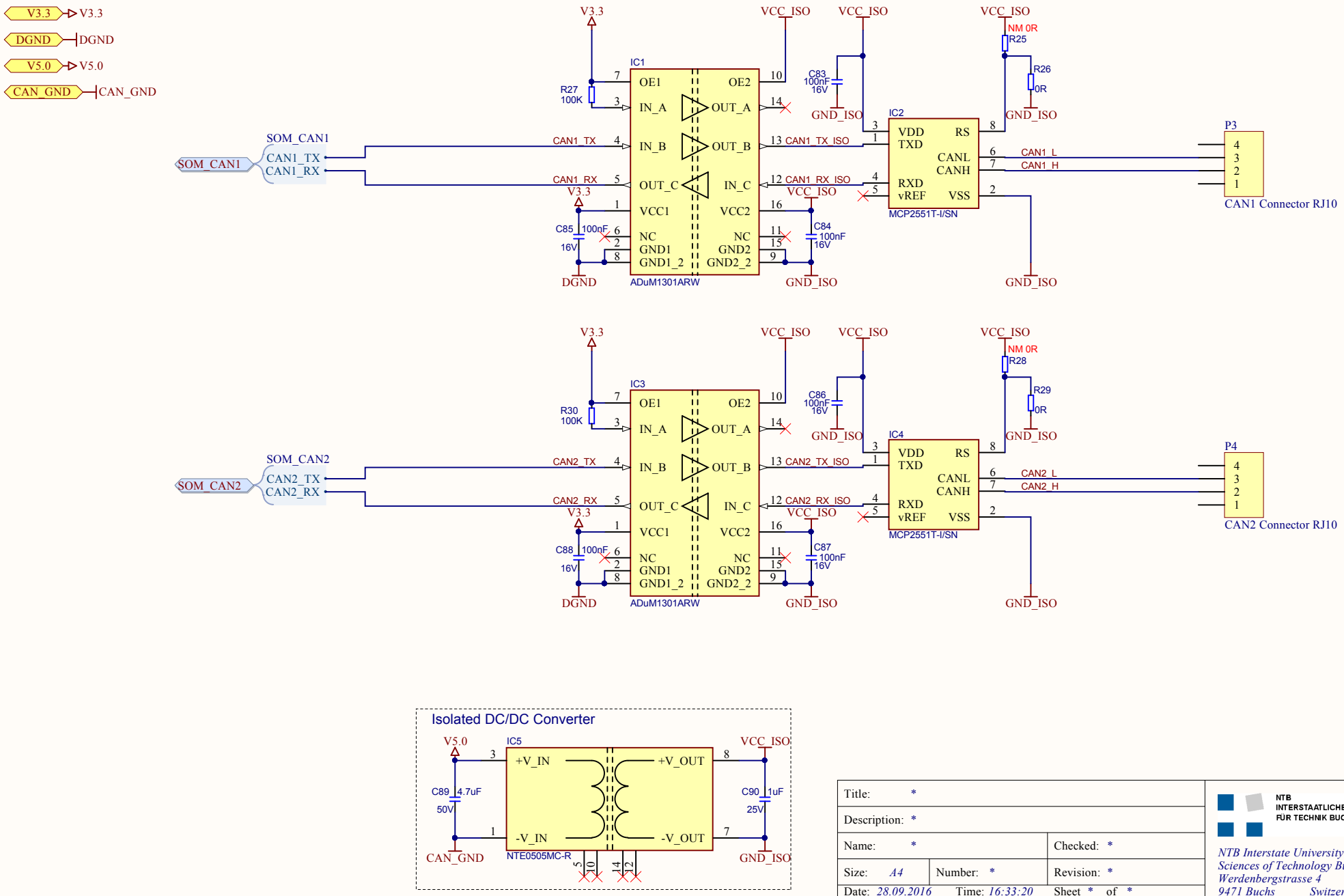

Title: *			
Description: *			
Name: *		Checked: *	
Size: A4	Number: *	Revision: *	
Date: 28.09.2016	Time: 16:33:20	Sheet * of *	
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_SOM_CAN.SchD			

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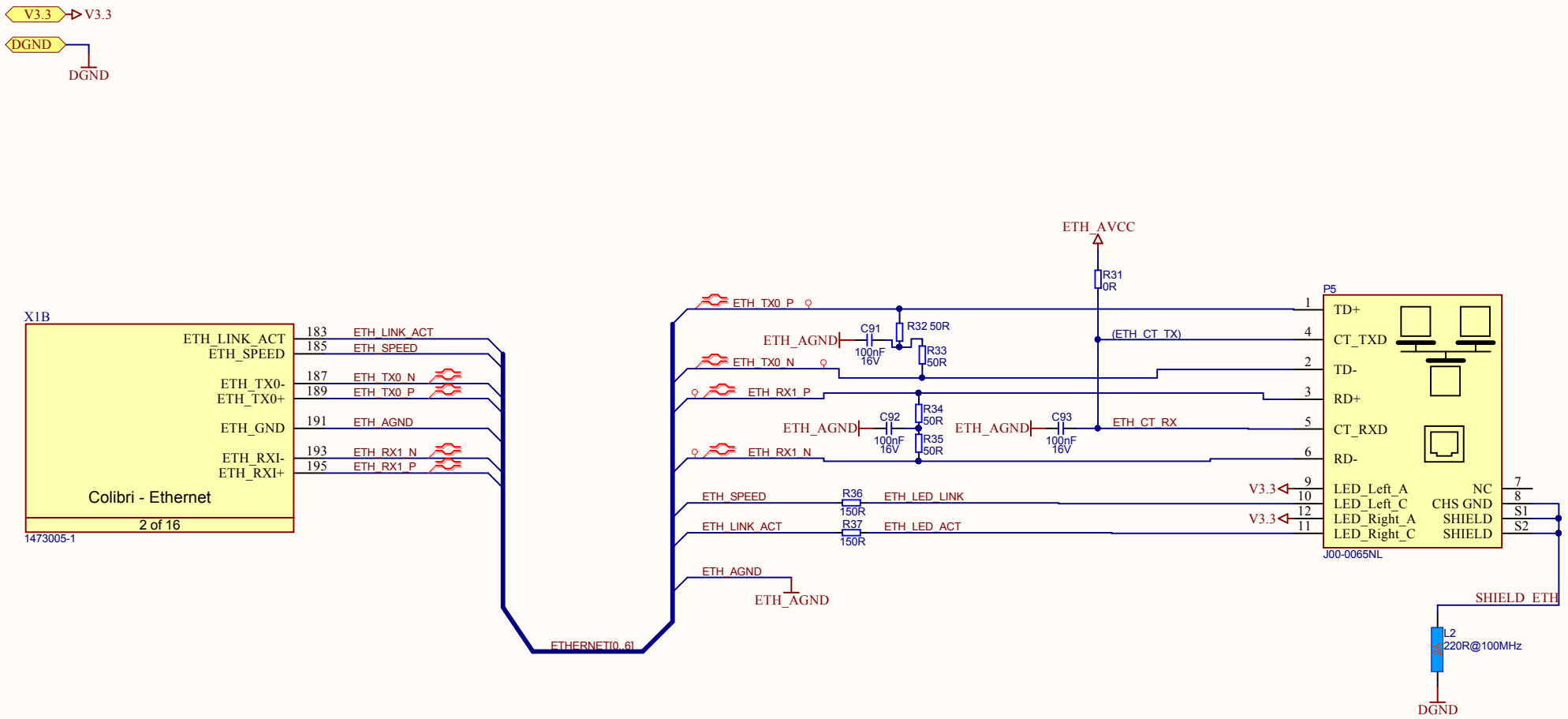

Title:	*Ethernet to SOM*		
Description:	*		
Name:	*A. Kalberer*		Checked: *
Size:	*A4*	Number: *	Revision: *
Date:	*28.09.2016*	Time: *16:33:20*	Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_SOM_Ethernet.S*		

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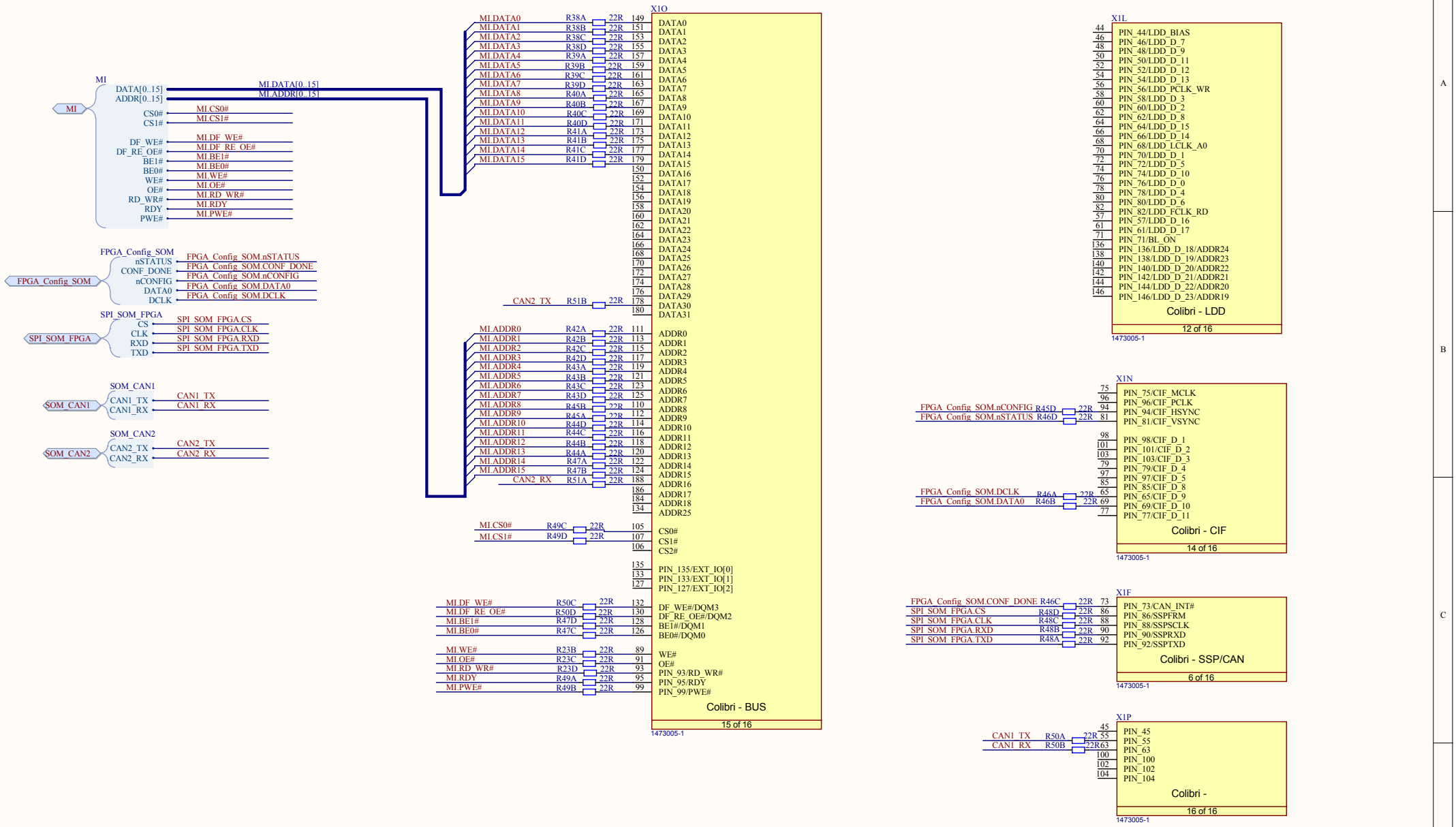

Title:	*EFS SOM IO*		
Description:	*SOM GMI-Bus, FPGA Config*		
Name:	*A. Kalberer*		Checked: *
Size:	*A3*	Number: *	Revision: *
Date:	*28.09.2016*	Time: *16:33:20*	Sheet * of *
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_SOM_IO.SchDoc*		

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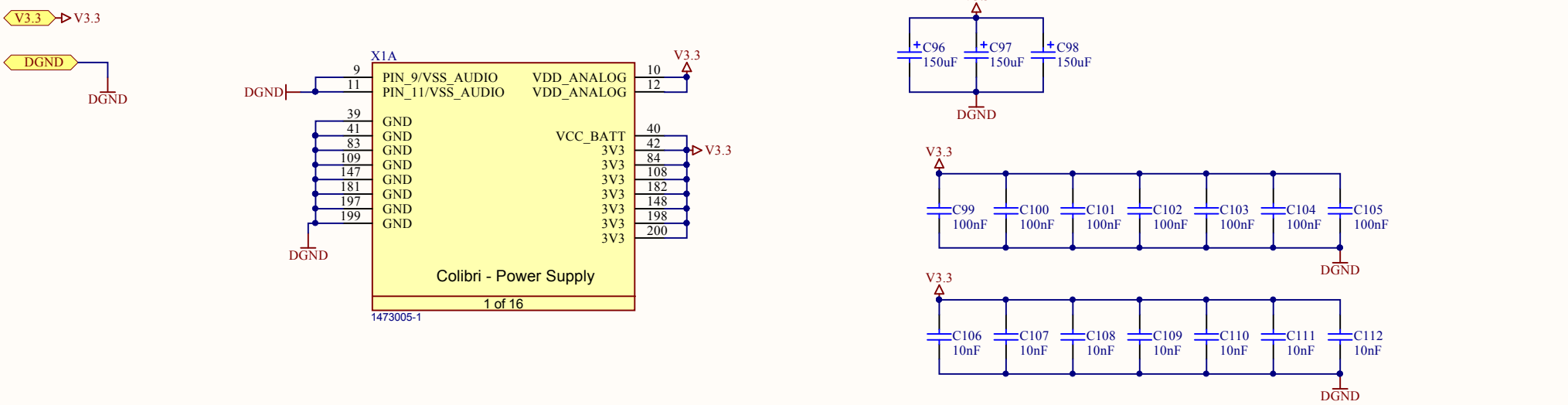

Title:	*SOM Power Supply*		
Description:	*		
Name:	*A. Kalberer*		Checked: *
Size:	*A4*	Number: *	Revision: *0.1*
Date:	*28.09.2016* Time: *16:33:20*	Sheet * of *	
File:	*D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\ControllerBoardExp\AltiumFiles\PATHOS_SOM_Power.Sch*		

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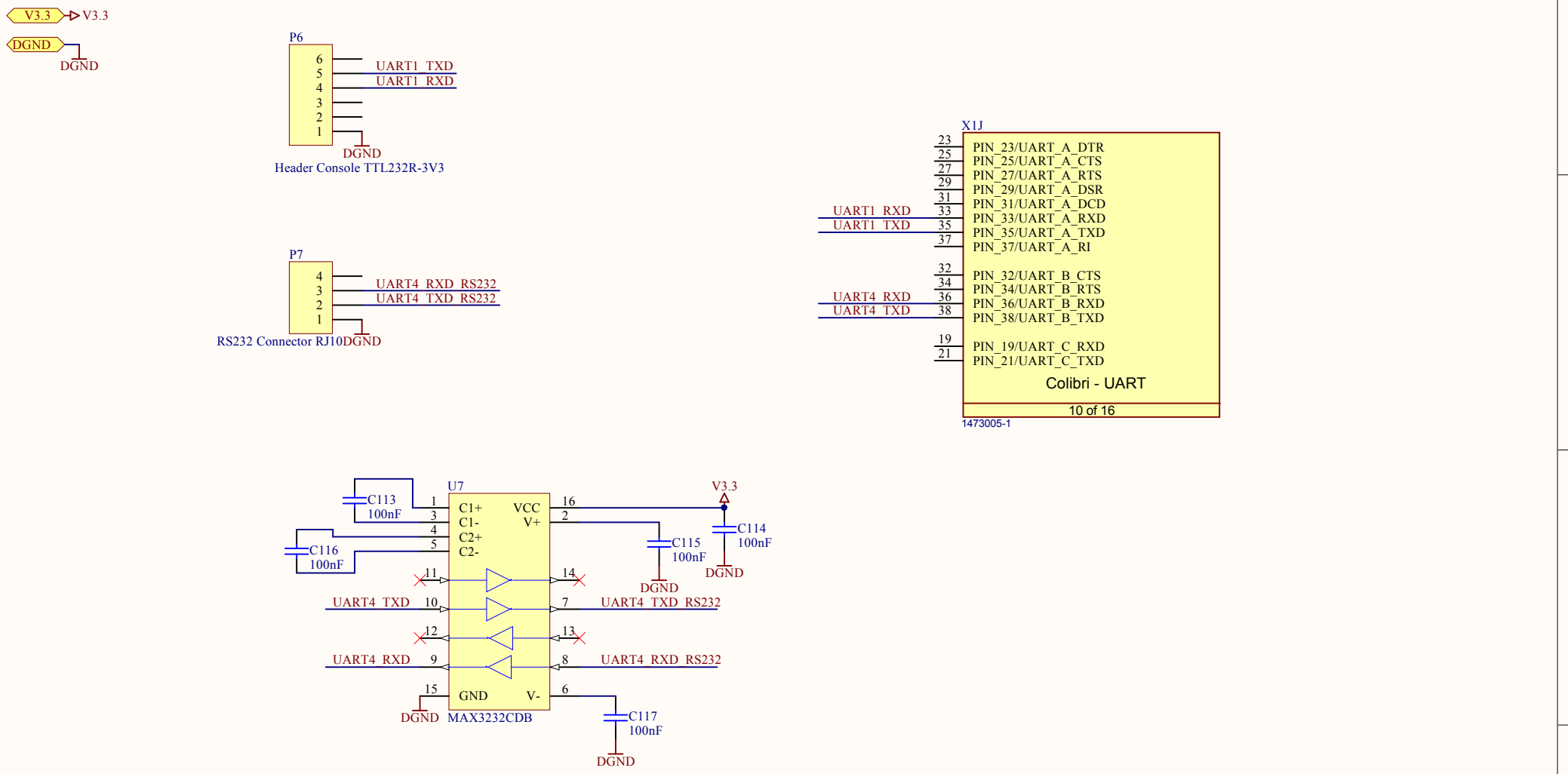

Title:	*UART Connectors*		
Description:			
Name:	*A. Kalberer*	Checked:	*
Size:	*A4*	Number: *	Revision: *
Date:	*28.09.2016* Time: *16:33:20*	Sheet * of *	
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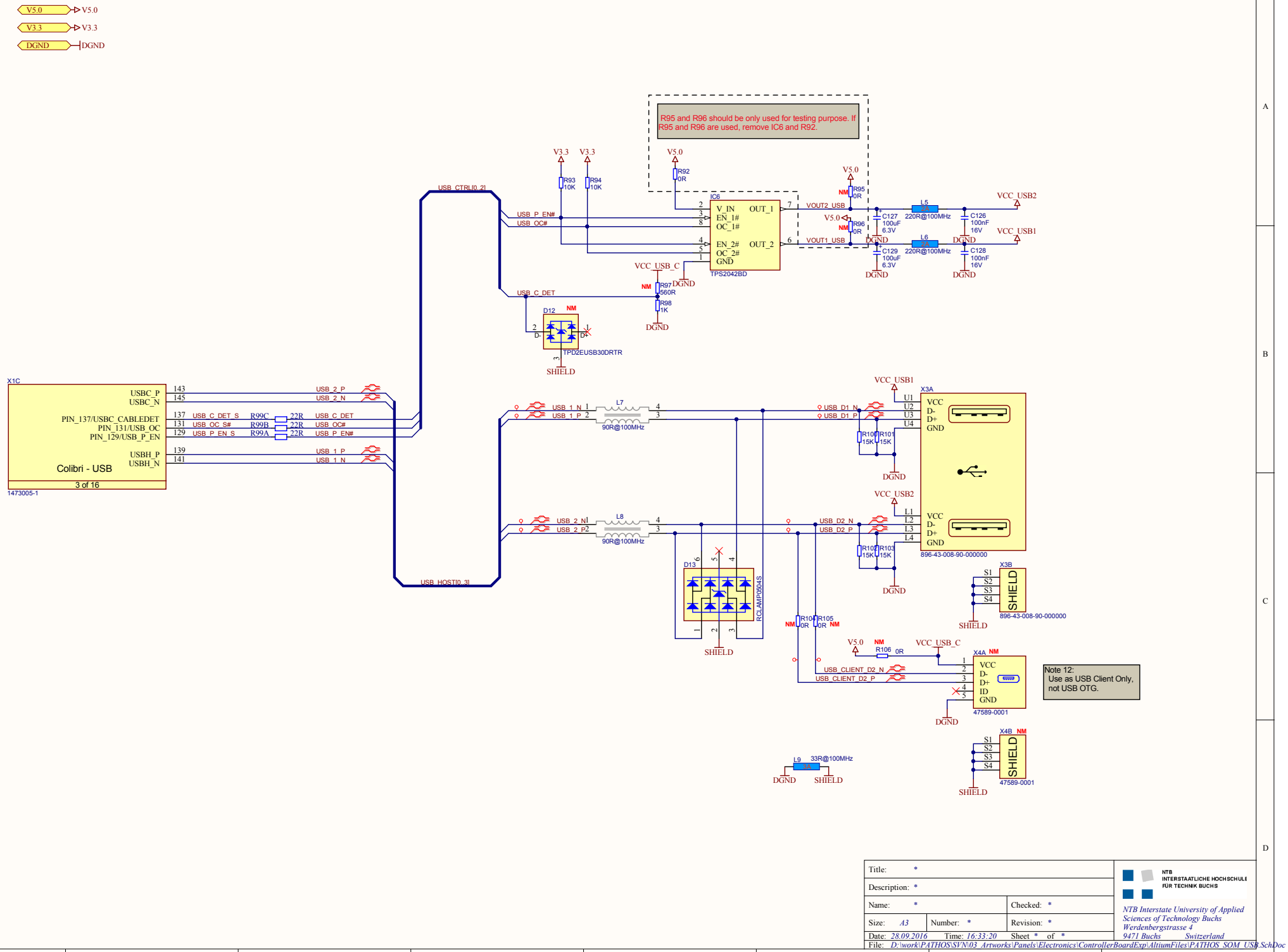
V5.0
V3.3
DGND
R95 and R96 should be only used for testing purpose. If R95 and R96 are used, remove IC6 and R92.
IC6
V_IN
EN_1#
OC_1#
EN_2#
OC_2#
GND
OUT_1
OUT_2
TPS2042BD
USB_CTRL[0..2]
USB_P_EN#
USB_OC#
USB_C_DET
VCC_USB_C
VOUT2_USB
VOUT1_USB
VCC_USB2
VCC_USB1
TPD2EUSB30DRTR
SHIELD
X1C
USBC_P
USBC_N
PIN_137/USBC_CABLEDET
PIN_131/USB_OC
PIN_129/USB_P_EN
USBH_P
USBH_N
Colibri - USB
3 of 16
1473005-1
USB_2_P
USB_2_N
USB_1_P
USB_1_N
USB_C_DET_S
USB_OC_S#
USB_P_EN_S
USB_HOST[0..3]
90R@100MHz
RCLAMP0604S
X3A
X3B
896-43-008-90-000000
X4A
X4B
47589-0001
Note 12:
Use as USB Client Only, not USB OTG.
L9
33R@100MHz
Title: *
Description: *
Name: *
Checked: *
Size: A3
Number: *
Revision: *
Date: 28.09.2016
Time: 16:33:20
Sheet * of *
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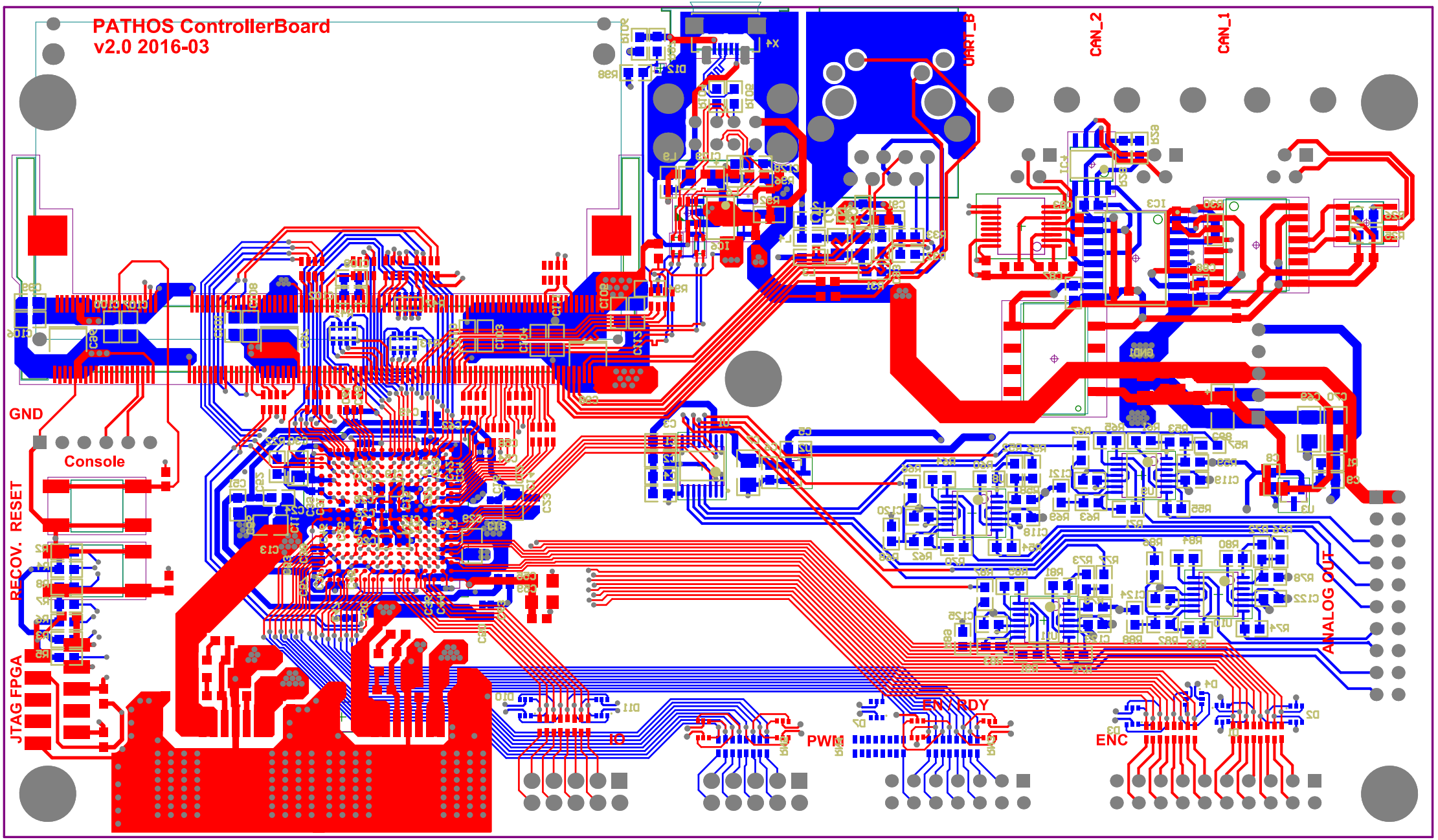
PATHOS ControllerBoard
v2.0 2016-03
UART_B
CAN_2
CAN_1
GND
Console
RECOV.
RESET
JTAG FPGA
IO
PWM
EN / RDY
ENC
ANALOG OUT