
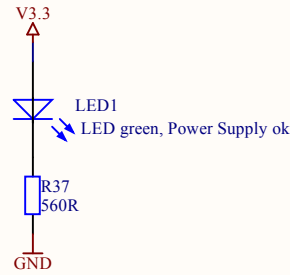
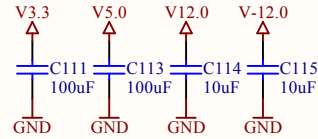
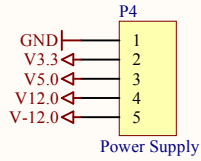
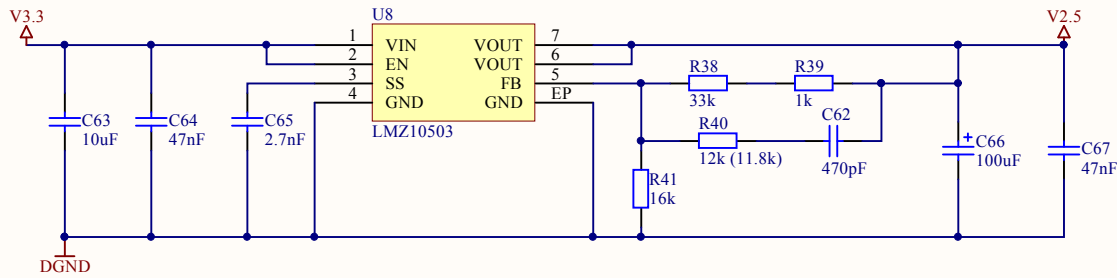


Title: <i>Main Schematic</i>		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS
Description:		
Name: <i>A. Kalberer</i>	Checked: *	
Size: <i>A4</i>	Number: *	Revision: <i>0.1</i>
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>	Sheet <i>1</i> of <i>2</i>
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_MainPCB.SchDoc</i>		

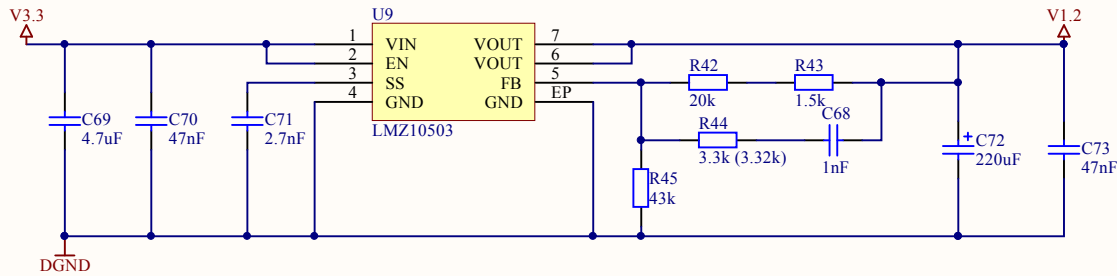
*NTB Interstate University of Applied Sciences of Technology Buchs*  
 Werdenbergstrasse 4  
 9471 Buchs Switzerland




Output: 2.5V max. 3A



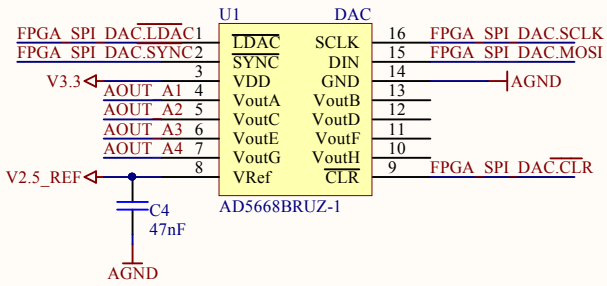
Output: 1.2V max. 3A



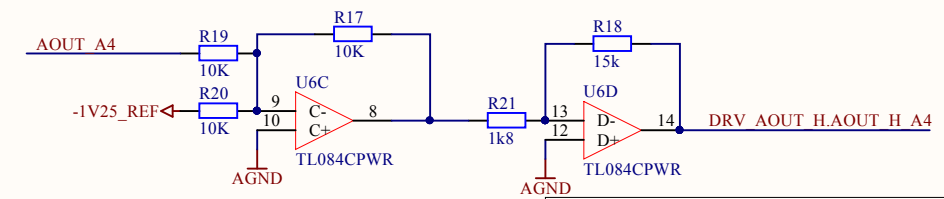
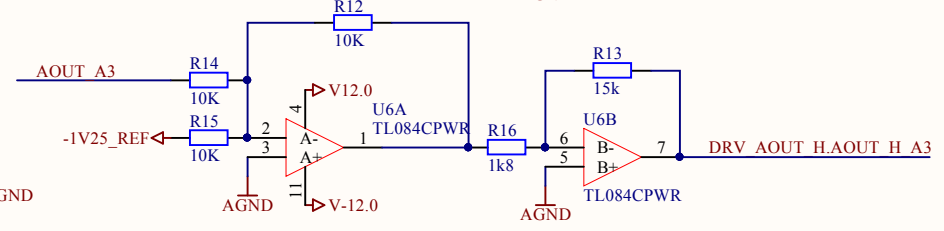
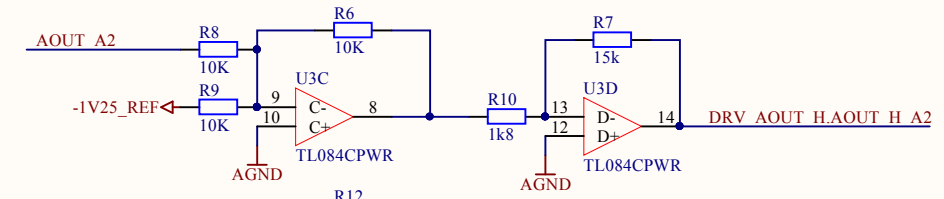
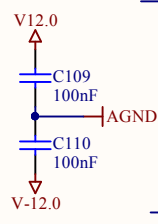
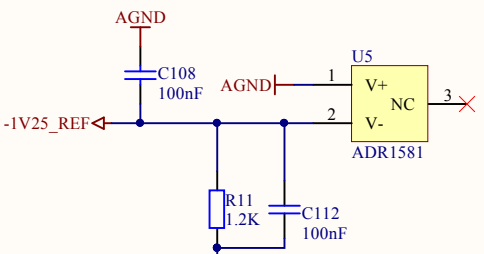
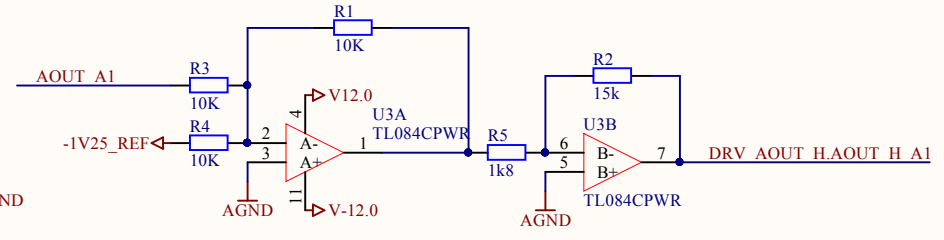
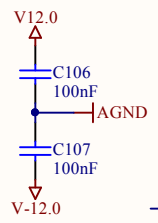
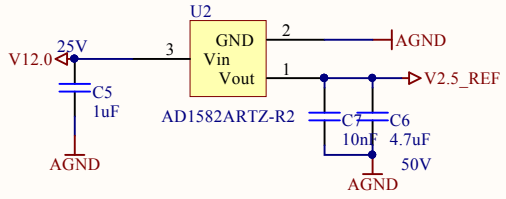
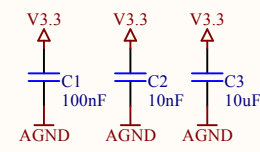
Title: <i>Power Supply Main PCB</i>		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS	
Description: <i>Power Supply</i>			
Name: <i>A. Kalberer</i>	Checked: *	<i>NTB Interstate University of Applied          Sciences of Technology Buchs          Werdenbergstrasse 4          9471 Buchs Switzerland</i>	
Size: <i>A4</i>	Number: *		Revision: <i>0.1</i>
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>		Sheet <i>2</i> of <i>2</i>
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_PowerSupply.SchDoc</i>			

V12.0 → V12.0  
 V-12.0 → V-12.0  
 AGND → AGND  
 V3.3 → V3.3

FPGA\_SPI\_DAC  
 MOSI → FPGA\_SPI\_DAC.MOSI  
 SCLK → FPGA\_SPI\_DAC.SCLK  
 SYNC → FPGA\_SPI\_DAC.SYNC  
 LDAC → FPGA\_SPI\_DAC.LDAC  
 CLR → FPGA\_SPI\_DAC.CLR



DRV\_AOUT\_H  
 AOUT\_H\_A1 → DRV\_AOUT\_H.AOUT\_H\_A1  
 AOUT\_H\_A2 → DRV\_AOUT\_H.AOUT\_H\_A2  
 AOUT\_H\_A3 → DRV\_AOUT\_H.AOUT\_H\_A3  
 AOUT\_H\_A4 → DRV\_AOUT\_H.AOUT\_H\_A4



Title: *		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS
Description: *		
Name: *		Checked: *
Size: A4	Number: *	Revision: *
Date: 09.12.2015	Time: 08:41:59	Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_AnalogOut.SchDoc		



1

2

3

4

A

A

B

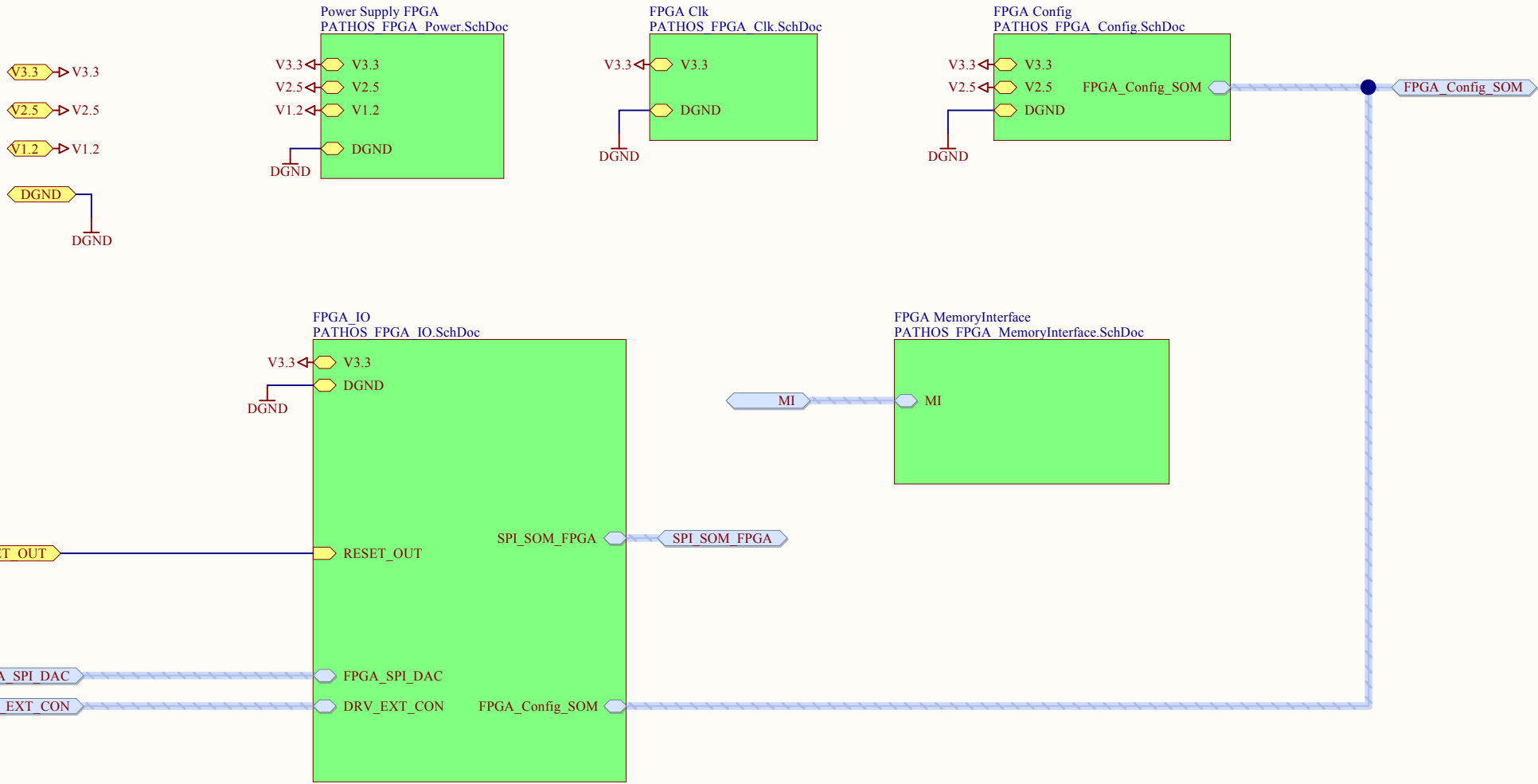
B


C

C

D

D



Title: <i>FPGA Overview</i>		 <b>NTB INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS</b>
Description:		
Name: <i>A. Kalberer</i>	Checked: *	
Size: <i>A4</i>	Number: *	Revision: <i>0.1</i>
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>	Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA.SchDoc</i>		

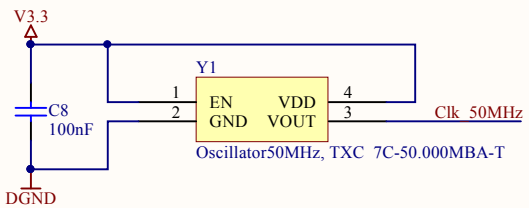
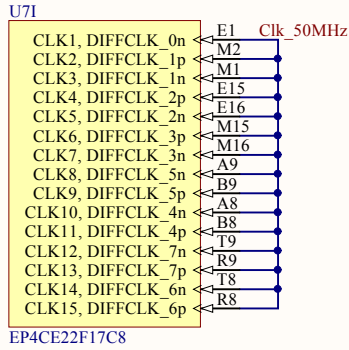
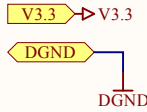
*NTB Interstate University of Applied  
Sciences of Technology Buchs  
Werdenbergstrasse 4  
9471 Buchs Switzerland*


1

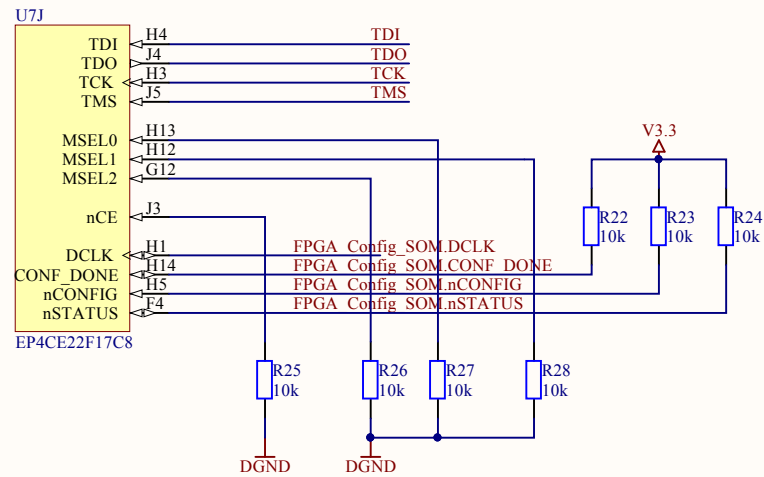
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3

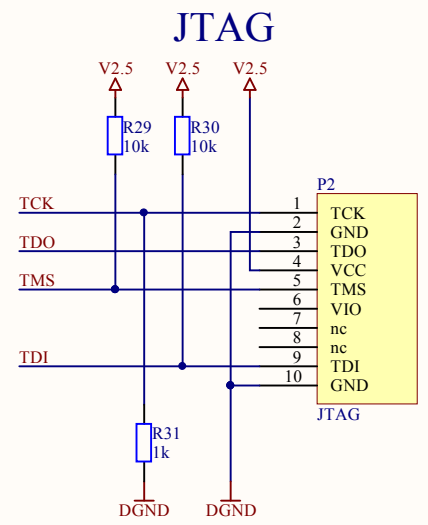
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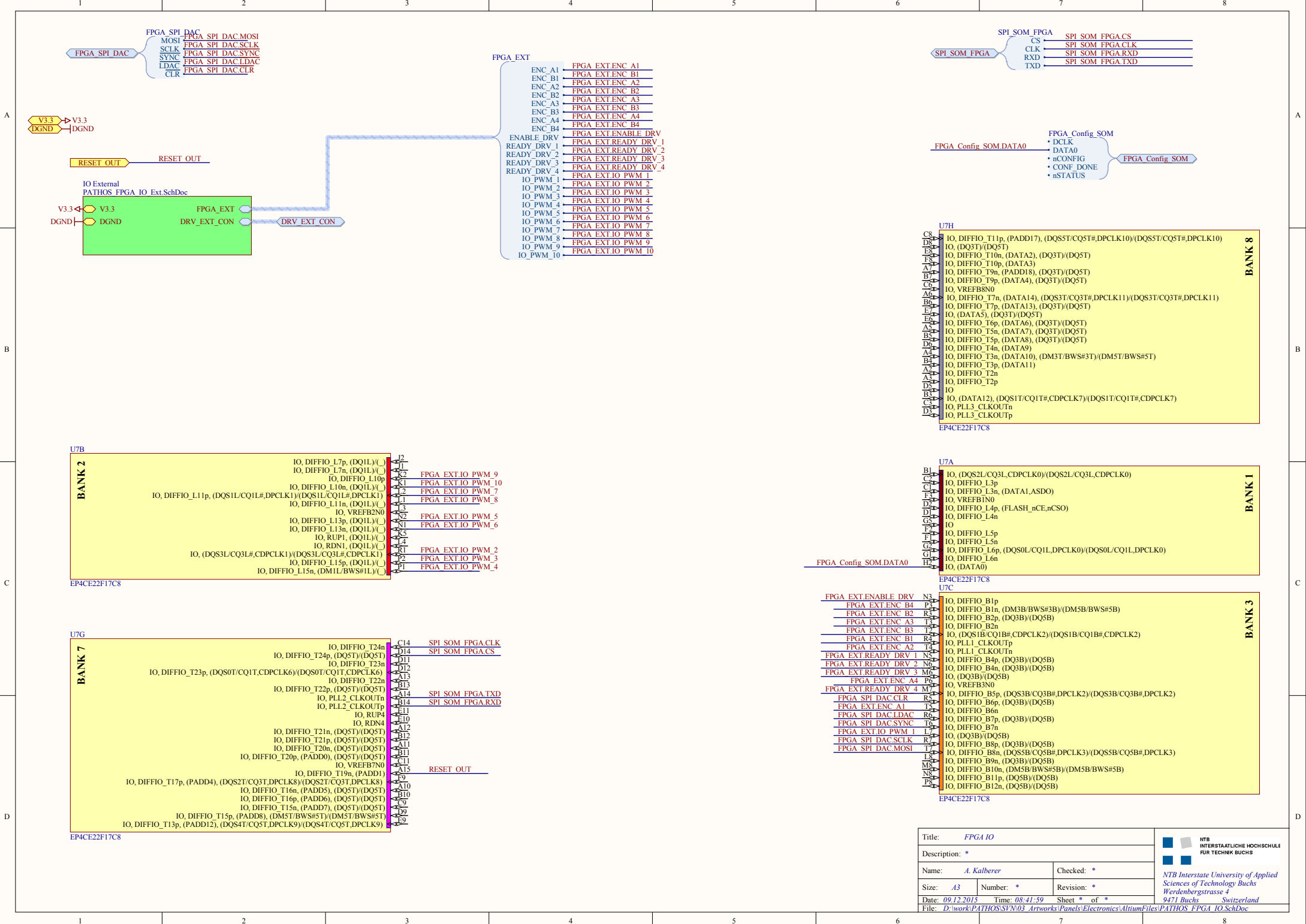
Title: <i>FPGA Clock</i>		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS  <i>NTB Interstate University of Applied          Sciences of Technology Buchs          Werdenbergstrasse 4          9471 Buchs Switzerland</i>
Description: *		
Name: <i>A. Kalberer</i>	Checked: *	
Size: <i>A4</i>	Number: *	
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>	Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA_Clk.SchDoc</i>		



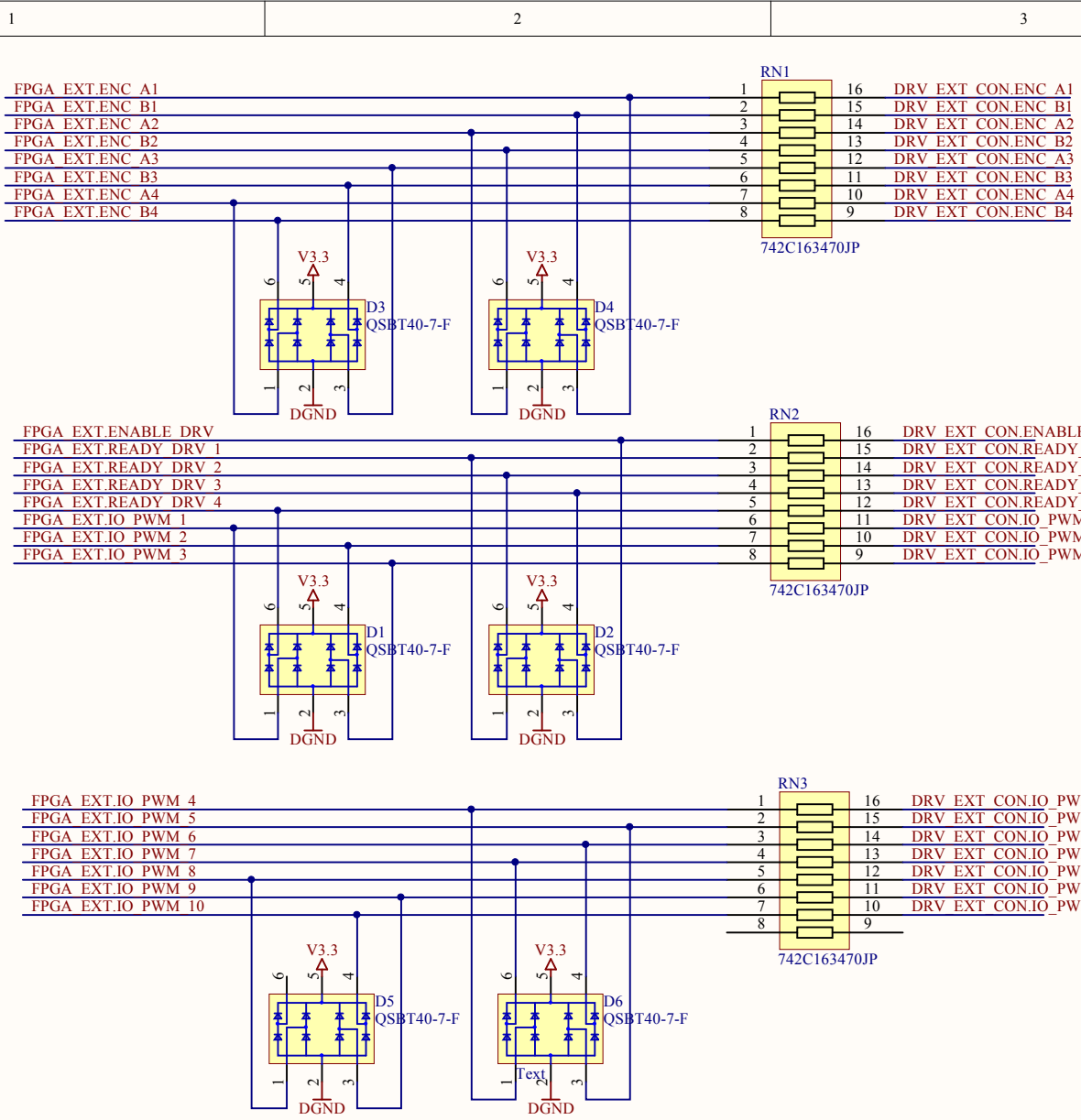
MSEL[0..2]: Config PS-Mode (0 0 0) see Cyclone IV Handbook page 173



Title: <i>FPGA Config</i>		 <b>NTB INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS</b>  <i>NTB Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland</i>	
Description:			
Name: <i>A. Kalberer</i>	Checked: *		
Size: <i>A4</i>	Number: *		Revision: *
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>		Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA_Config.SchDoc</i>			







FPGA\_EXT

ENC_A1	FPGA_EXT.ENC_A1
ENC_B1	FPGA_EXT.ENC_B1
ENC_A2	FPGA_EXT.ENC_A2
ENC_B2	FPGA_EXT.ENC_B2
ENC_A3	FPGA_EXT.ENC_A3
ENC_B3	FPGA_EXT.ENC_B3
ENC_A4	FPGA_EXT.ENC_A4
ENC_B4	FPGA_EXT.ENC_B4
ENABLE_DRV	FPGA_EXT.ENABLE_DRV
READY_DRV_1	FPGA_EXT.READY_DRV_1
READY_DRV_2	FPGA_EXT.READY_DRV_2
READY_DRV_3	FPGA_EXT.READY_DRV_3
READY_DRV_4	FPGA_EXT.READY_DRV_4
IO_PWM_1	FPGA_EXT.IO_PWM_1
IO_PWM_2	FPGA_EXT.IO_PWM_2
IO_PWM_3	FPGA_EXT.IO_PWM_3
IO_PWM_4	FPGA_EXT.IO_PWM_4
IO_PWM_5	FPGA_EXT.IO_PWM_5
IO_PWM_6	FPGA_EXT.IO_PWM_6
IO_PWM_7	FPGA_EXT.IO_PWM_7
IO_PWM_8	FPGA_EXT.IO_PWM_8
IO_PWM_9	FPGA_EXT.IO_PWM_9
IO_PWM_10	FPGA_EXT.IO_PWM_10

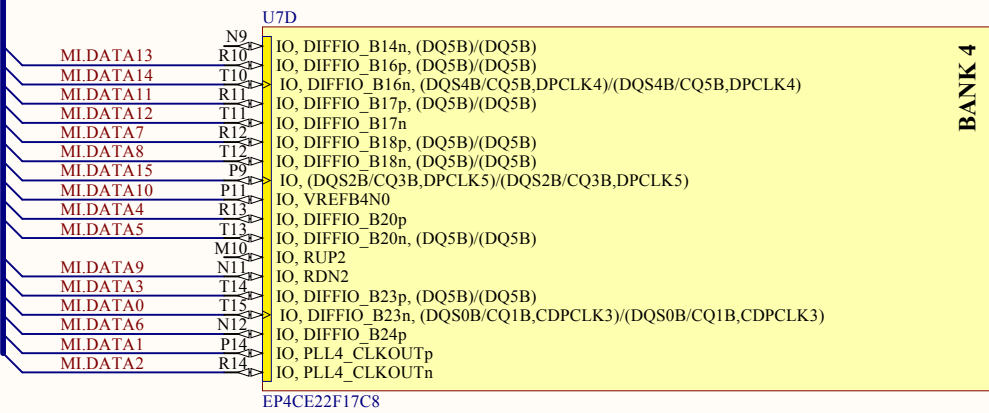
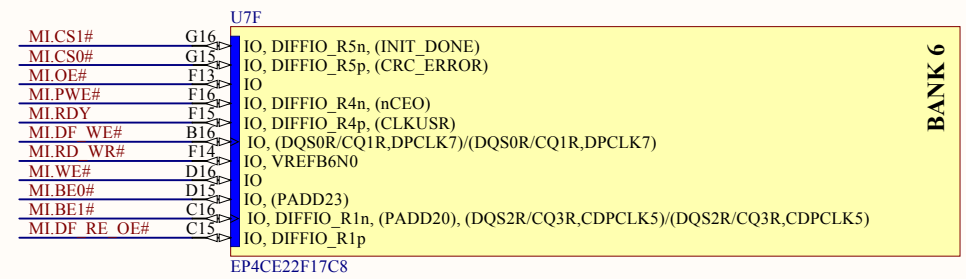
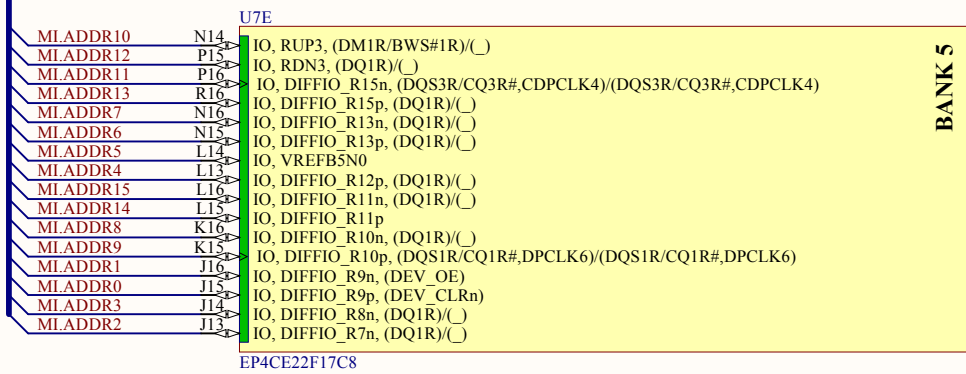
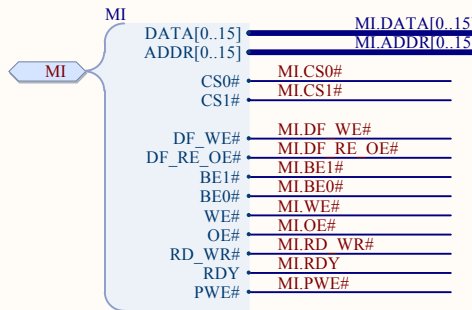
DRV\_EXT\_CON


ENC_A1	DRV_EXT_CON.ENC_A1
ENC_B1	DRV_EXT_CON.ENC_B1
ENC_A2	DRV_EXT_CON.ENC_A2
ENC_B2	DRV_EXT_CON.ENC_B2
ENC_A3	DRV_EXT_CON.ENC_A3
ENC_B3	DRV_EXT_CON.ENC_B3
ENC_A4	DRV_EXT_CON.ENC_A4
ENC_B4	DRV_EXT_CON.ENC_B4
ENABLE_DRV	DRV_EXT_CON.ENABLE_DRV
READY_DRV_1	DRV_EXT_CON.READY_DRV_1
READY_DRV_2	DRV_EXT_CON.READY_DRV_2
READY_DRV_3	DRV_EXT_CON.READY_DRV_3
READY_DRV_4	DRV_EXT_CON.READY_DRV_4
IO_PWM_1	DRV_EXT_CON.IO_PWM_1
IO_PWM_2	DRV_EXT_CON.IO_PWM_2
IO_PWM_3	DRV_EXT_CON.IO_PWM_3
IO_PWM_4	DRV_EXT_CON.IO_PWM_4
IO_PWM_5	DRV_EXT_CON.IO_PWM_5
IO_PWM_6	DRV_EXT_CON.IO_PWM_6
IO_PWM_7	DRV_EXT_CON.IO_PWM_7
IO_PWM_8	DRV_EXT_CON.IO_PWM_8
IO_PWM_9	DRV_EXT_CON.IO_PWM_9
IO_PWM_10	DRV_EXT_CON.IO_PWM_10

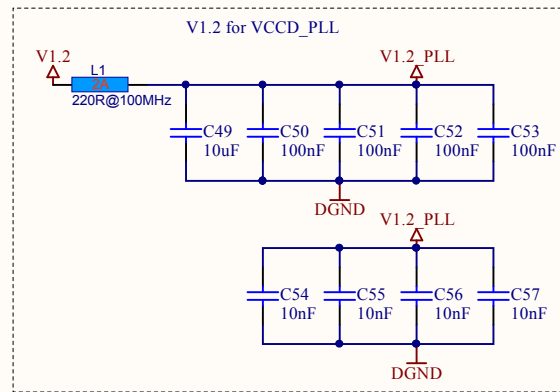
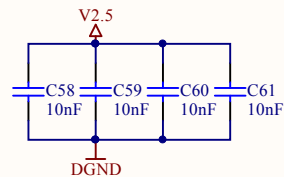
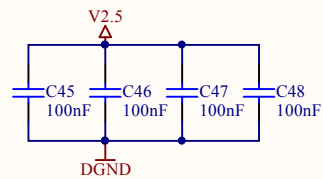
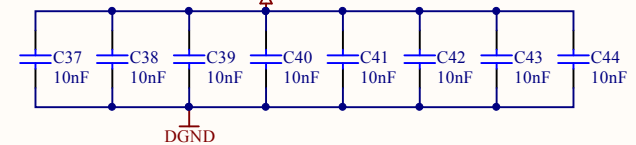
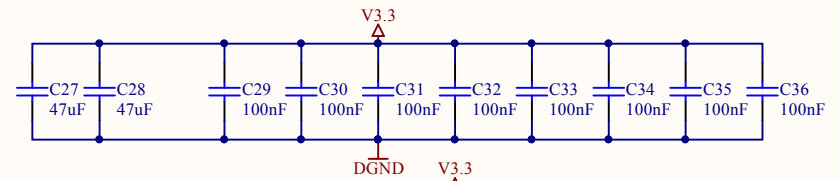
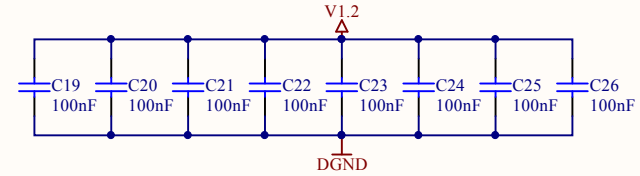
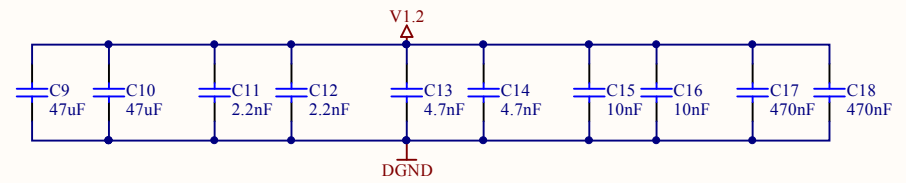
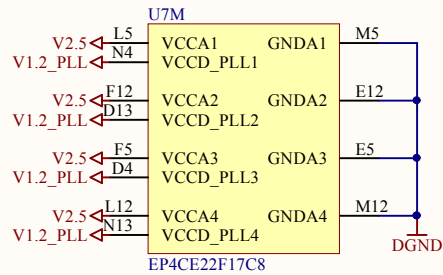
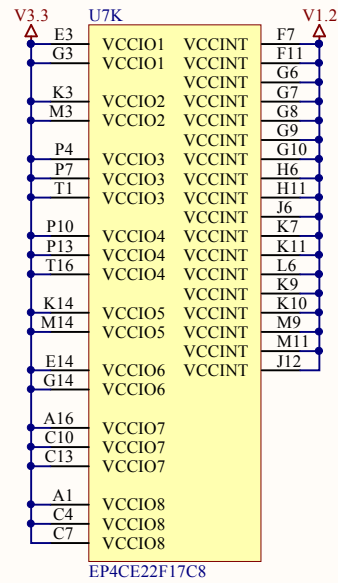
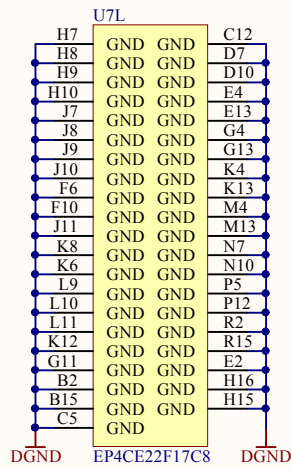
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Description:	*				
Name:	*	Checked:	*		
Size:	A4	Number:	*	Revision:	*
Date:	09.12.2015	Time:	08:41:59	Sheet	* of *
File:	D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA_IO_Ext.SchDoc				


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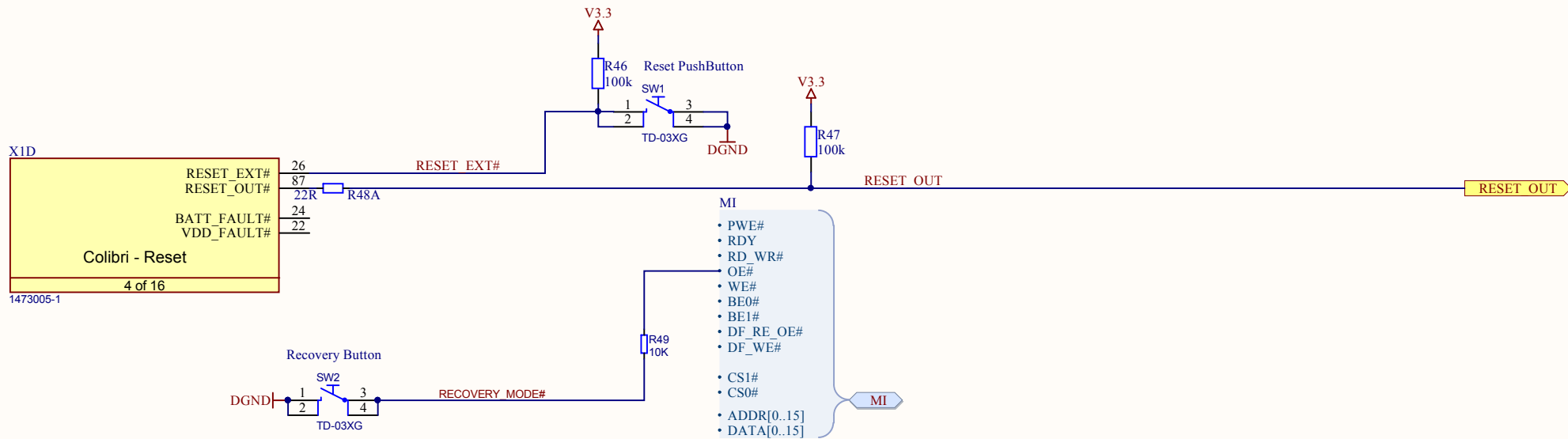
NTB Interstate University of Applied  
Sciences of Technology Buchs  
Werdenbergstrasse 4  
9471 Buchs Switzerland




Title: <i>FPGA SOM Memory Interface</i>		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS	
Description: *			
Name: <i>A. Kalberer</i>	Checked: *	<i>NTB</i> Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland	
Size: <i>A4</i>	Number: *		Revision: *
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>		Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA_MemoryInterface.SchDoc</i>			



Title: <i>FPGA Power</i>		 <b>NTB INTERSTÄATLICHE HOCHSCHULE FÜR TECHNIK BUCHS</b>  <i>NTB Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland</i>
Description:		
Name: <i>A. Kalberer</i>	Checked: *	
Size: <i>A4</i>	Number: *	
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>	Revision: *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_FPGA_Power.SchDoc</i>		Sheet * of *



Title: <i>Power Switch Schematic</i>		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS	
Description: <i>Power-, Reset-, Recovery-Circuit</i>			
Name: <i>A. Kalberer</i>	Checked: *	<i>NTB Interstate University of Applied          Sciences of Technology Buchs          Werdenbergstrasse 4          9471 Buchs Switzerland</i>	
Size: <i>A4</i>	Number: *		Revision: *
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>		Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_PowerSwitch.SchDoc</i>			

1

2

3

4

A

A

B

B

C

C

D

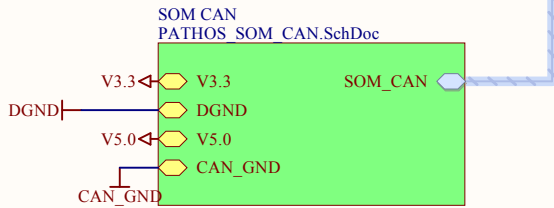
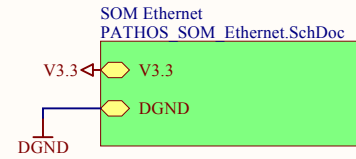
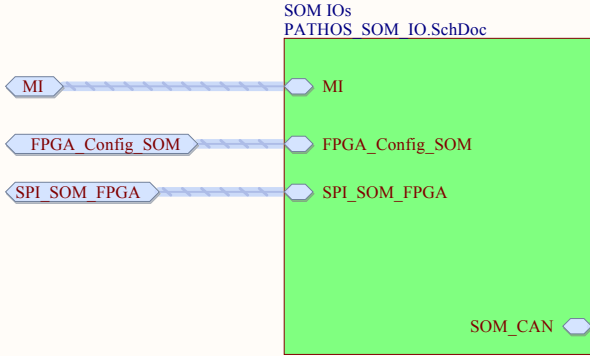
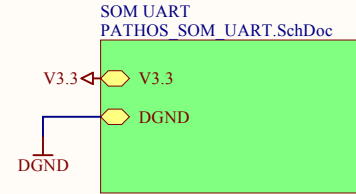
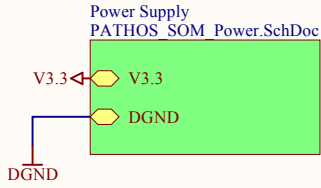
D


V3.3 → V3.3

DGND → DGND

V5.0 → V5.0

CAN\_GND → CAN\_GND



Title: <i>SOM Main Schematic</i>		 <b>NTB INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS</b>		
Description:				
Name: <i>A. Kalberer</i>	Checked: *	<i>NTB Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland</i>		
Size: <i>A4</i>	Number: *			Revision: *
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>			Sheet * of *
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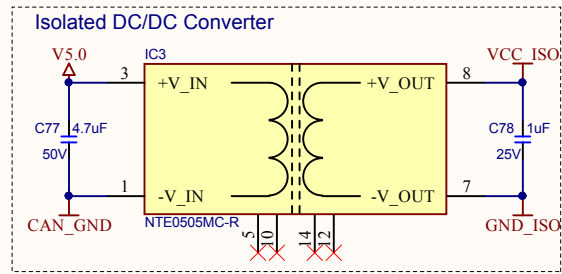
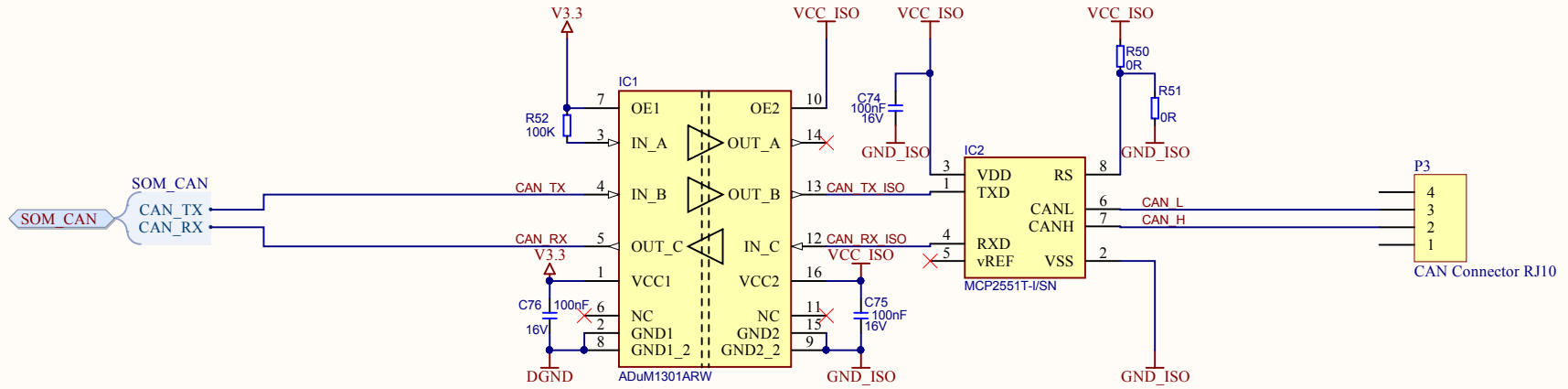
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2

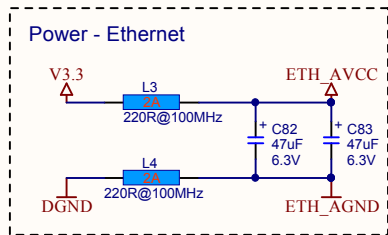
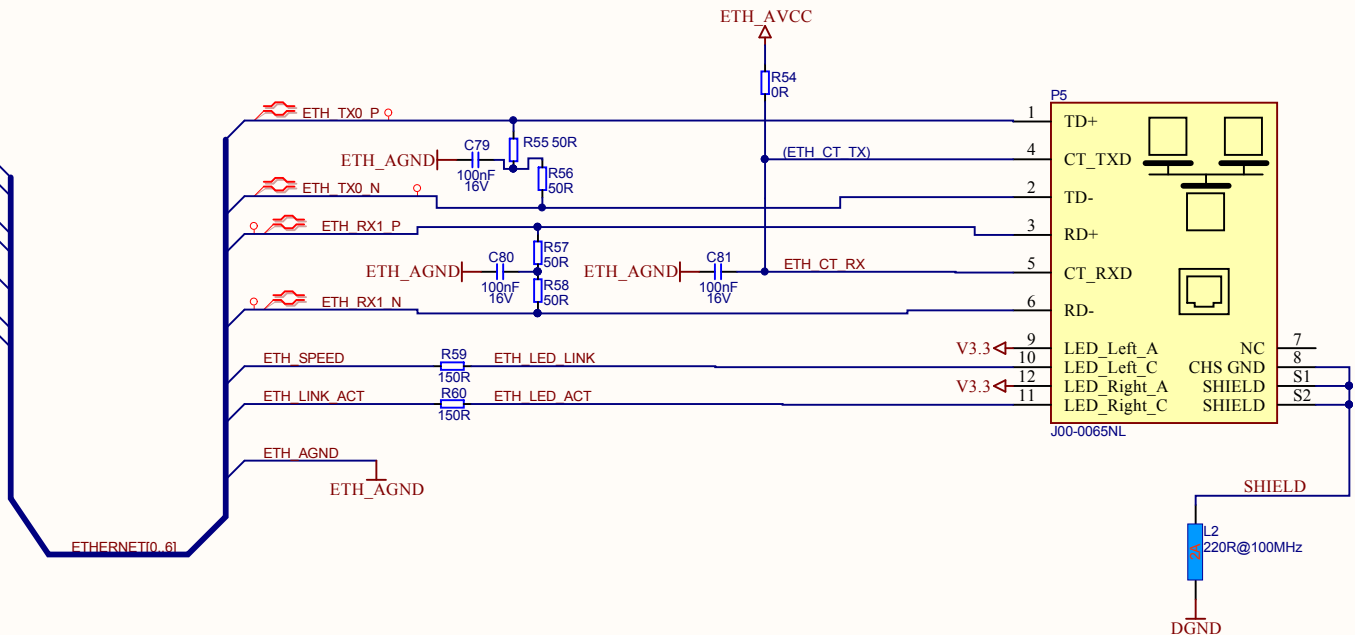
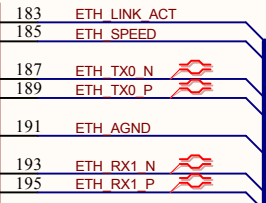
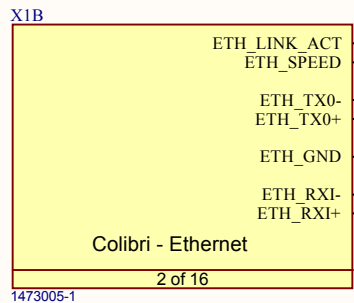
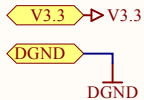
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4

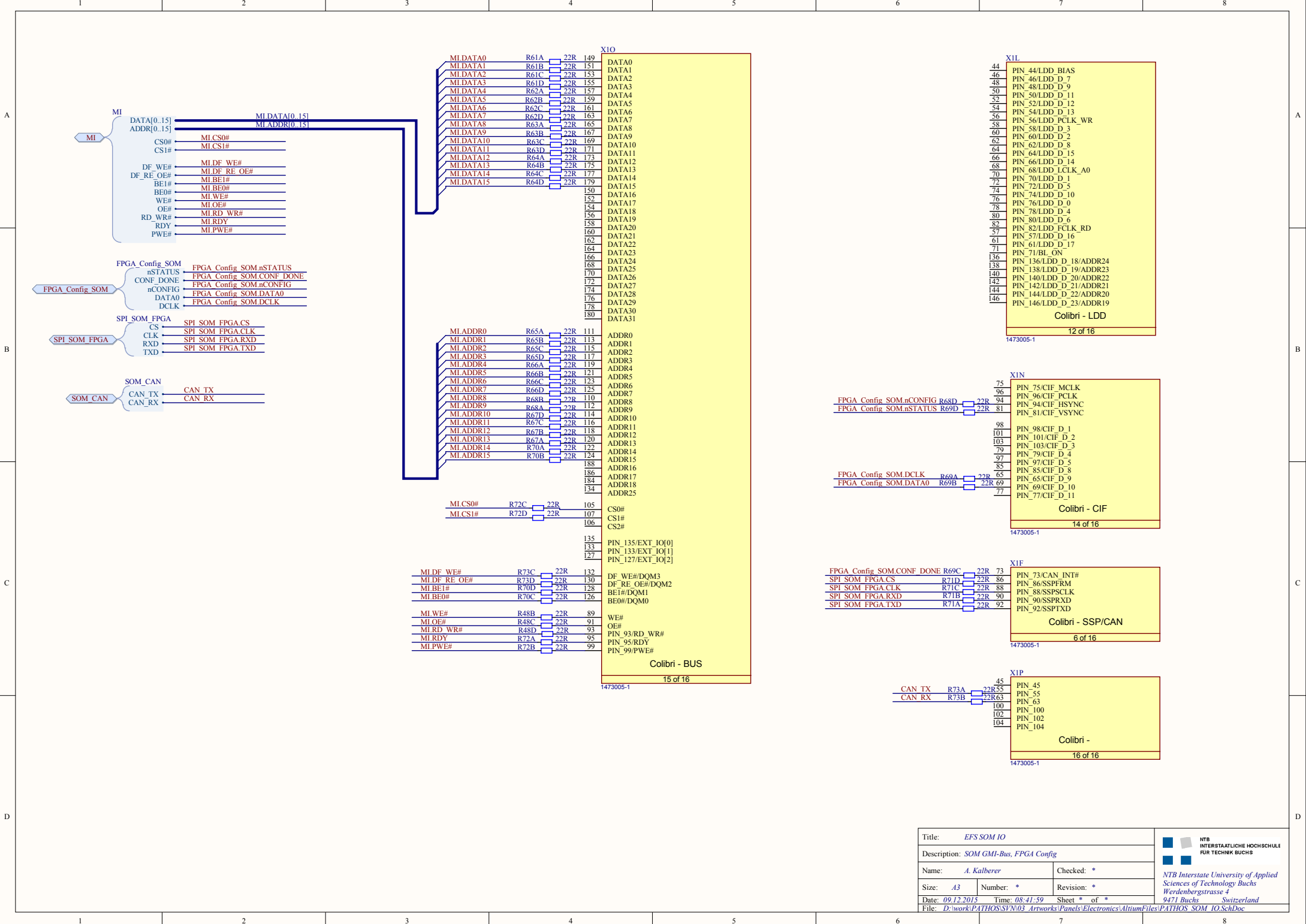
-  V3.3
-  DGND
-  V5.0
-  CAN\_GND



Title: *		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS  <i>NTB Interstate University of Applied          Sciences of Technology Buchs          Werdenbergstrasse 4          9471 Buchs Switzerland</i>
Description: *		
Name: *	Checked: *	
Size: A4	Number: *	
Date: 09.12.2015	Time: 08:41:59	Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_SOM_CAN.SchDoc		



Title: Ethernet to SOM		 <b>NTB</b> INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS  <i>NTB Interstate University of Applied          Sciences of Technology Buchs          Werdenbergstrasse 4          9471 Buchs Switzerland</i>
Description: *		
Name: A. Kalberer	Checked: *	
Size: A4	Number: * Revision: *	
Date: 09.12.2015	Time: 08:41:59	Sheet * of *
File: D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_SOM_Ethernet.SchDoc		



Title: EFS SOM IO	
Description: SOM GMI-Bus, FPGA Config	
Name: A. Kalberer	Checked: *
Size: A3	Number: *
Date: 09.12.2013	Time: 08:41:59
File: D:\work\PATHOS\SN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_SOM_IO.SchDoc	Sheet * of *


**NTB**  
 INTERSTAATLICHE HOCHSCHULE  
 FÜR TECHNIK BUCHS  
 NTB Interstate University of Applied  
 Sciences of Technology Buchs  
 Werdenbergstrasse 4  
 9471 Buchs Switzerland

A

A

B

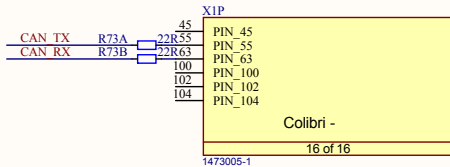
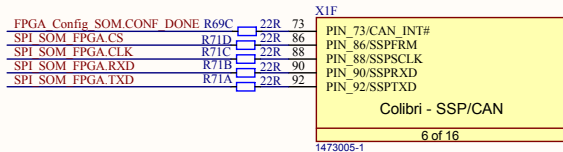
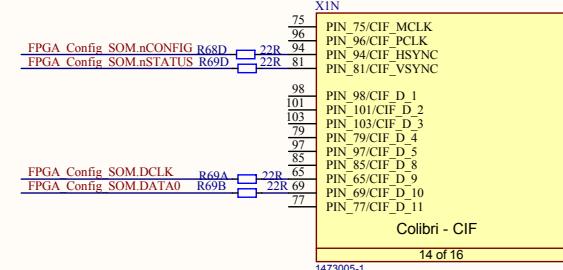
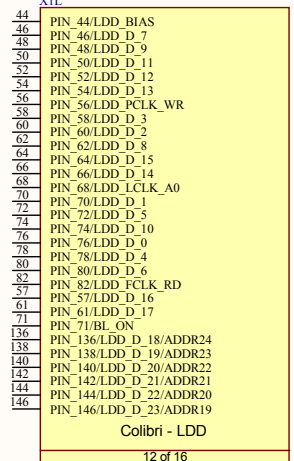
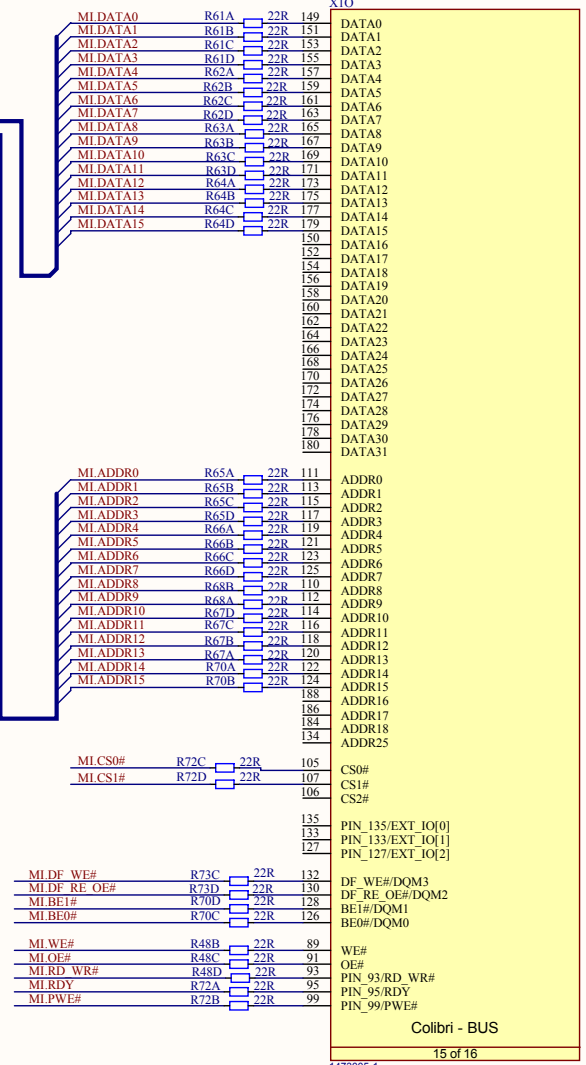
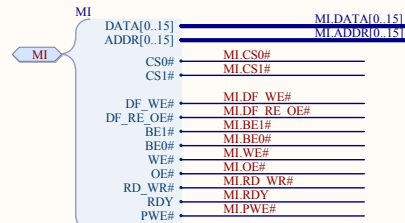
B

C

C

D

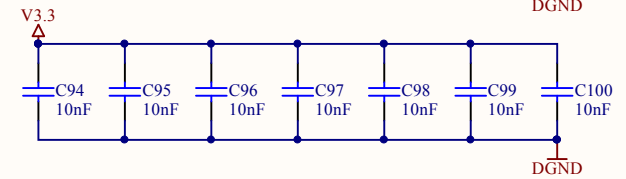
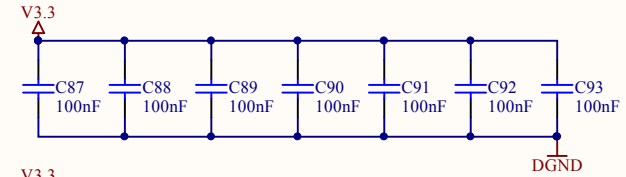
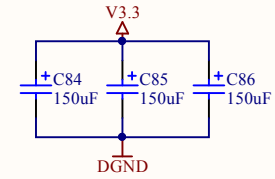
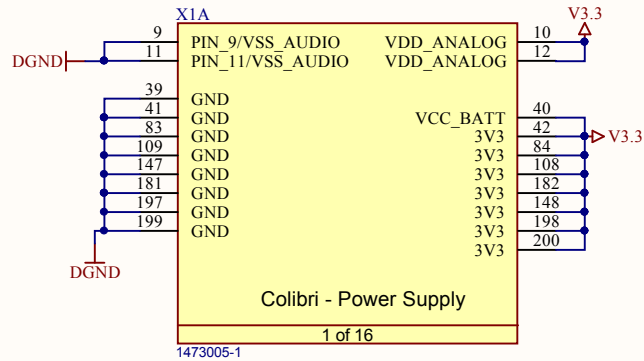
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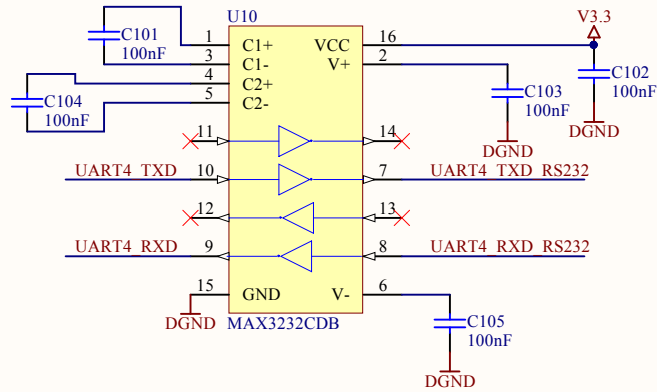
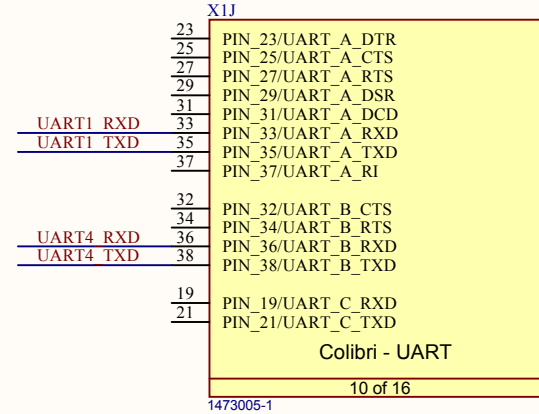
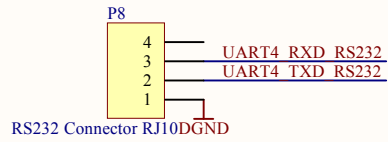
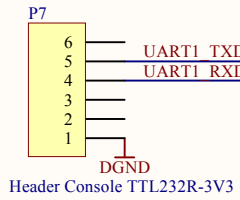


V3.3 → V3.3

DGND → DGND



Title: <i>SOM Power Supply</i>		 NTB INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS	
Description: *			
Name: <i>A. Kalberer</i>	Checked: *	<i>NTB Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland</i>	
Size: <i>A4</i>	Number: *		Revision: <i>0.1</i>
Date: <i>09.12.2015</i>	Time: <i>08:41:59</i>		Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_SOM_Power.SchDoc</i>			



Title: <i>UART Connectors</i>		 NTB INTERSTAATLICHE HOCHSCHULE FÜR TECHNIK BUCHS  <i>NTB Interstate University of Applied Sciences of Technology Buchs Werdenbergstrasse 4 9471 Buchs Switzerland</i>
Description:		
Name: <i>A. Kalberer</i>	Checked: *	
Size: <i>A4</i>	Number: * Revision: *	
Date: <i>09.12.2015</i>	Time: <i>08:42:00</i>	Sheet * of *
File: <i>D:\work\PATHOS\SVN\03_Artworks\Panels\Electronics\AltiumFiles\PATHOS_SOM_UART.SchDoc</i>		

