

Zynq MicroZed	
Avnet Engineering Services	
www.microzed.org	
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MicroZed_Production

12 Dec 2014

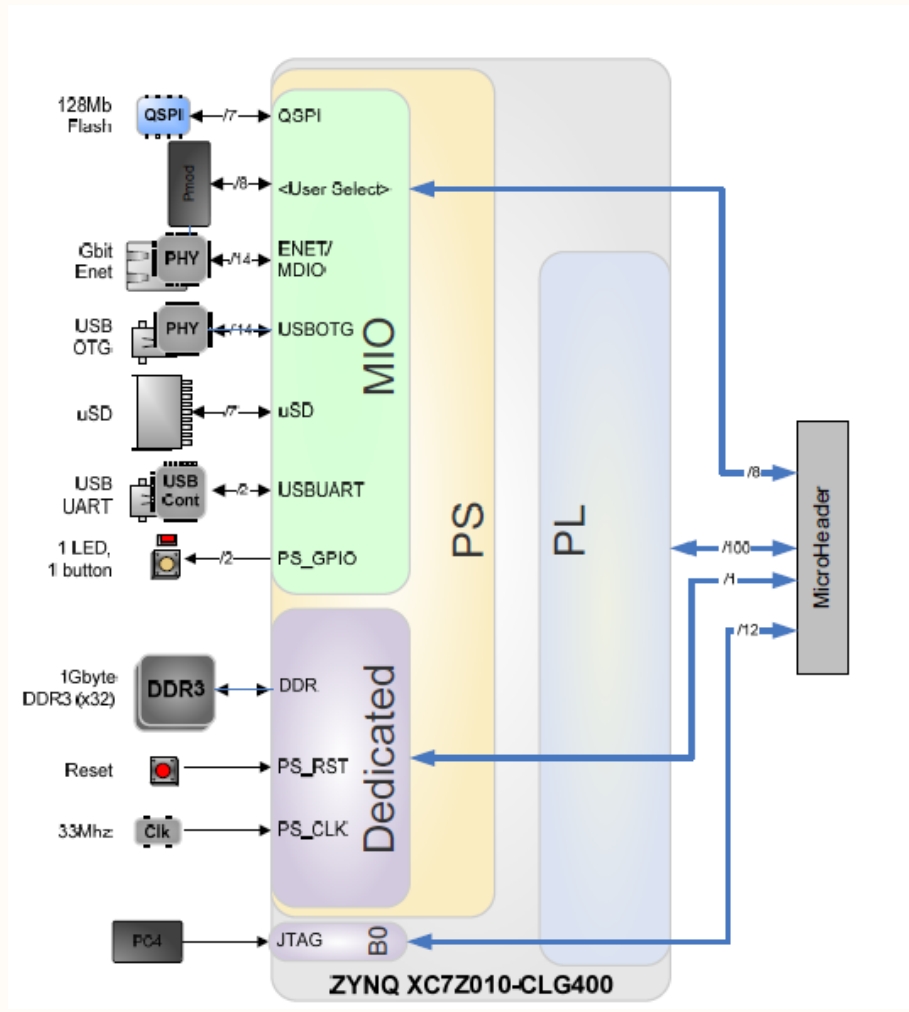
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Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_B.SchDoc		
Size: B	Document Number: MicroZed 7010	Rev: F-06
Date: 12/10/2014	Sheet 1 of 11	

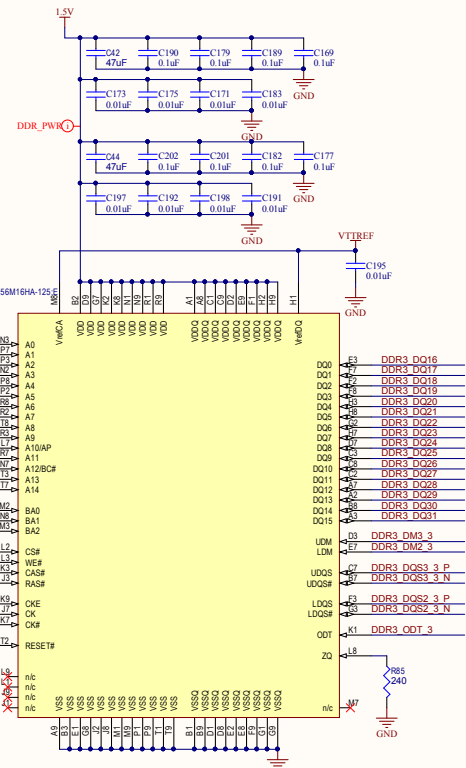
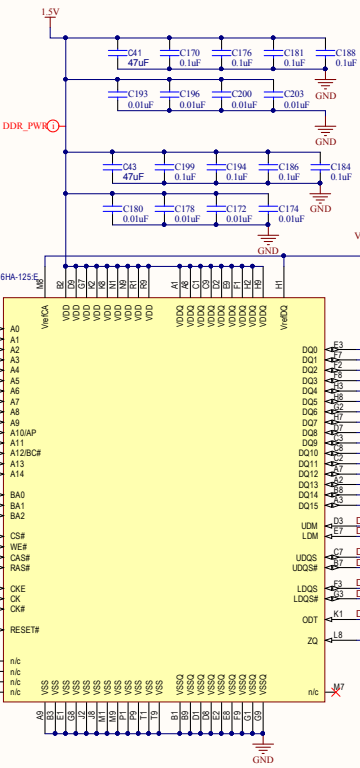


 Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: B	Document Number:	Rev: F-06
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BANK 502

PS_DDR_DQ0_502	DDR3 DQ0
PS_DDR_DQ1_502	DDR3 DQ1
PS_DDR_DQ2_502	DDR3 DQ2
PS_DDR_DQ3_502	DDR3 DQ3
PS_DDR_DQ4_502	DDR3 DQ4
PS_DDR_DQ5_502	DDR3 DQ5
PS_DDR_DQ6_502	DDR3 DQ6
PS_DDR_DQ7_502	DDR3 DQ7
PS_DDR_DQ8_502	DDR3 DQ8
PS_DDR_DQ9_502	DDR3 DQ9
PS_DDR_DQ10_502	DDR3 DQ10
PS_DDR_DQ11_502	DDR3 DQ11
PS_DDR_DQ12_502	DDR3 DQ12
PS_DDR_DQ13_502	DDR3 DQ13
PS_DDR_DQ14_502	DDR3 DQ14
PS_DDR_DQ15_502	DDR3 DQ15
PS_DDR_DQ16_502	DDR3 DQ16
PS_DDR_DQ17_502	DDR3 DQ17
PS_DDR_DQ18_502	DDR3 DQ18
PS_DDR_DQ19_502	DDR3 DQ19
PS_DDR_DQ20_502	DDR3 DQ20
PS_DDR_DQ21_502	DDR3 DQ21
PS_DDR_DQ22_502	DDR3 DQ22
PS_DDR_DQ23_502	DDR3 DQ23
PS_DDR_DQ24_502	DDR3 DQ24
PS_DDR_DQ25_502	DDR3 DQ25
PS_DDR_DQ26_502	DDR3 DQ26
PS_DDR_DQ27_502	DDR3 DQ27
PS_DDR_DQ28_502	DDR3 DQ28
PS_DDR_DQ29_502	DDR3 DQ29
PS_DDR_DQ30_502	DDR3 DQ30
PS_DDR_DQ31_502	DDR3 DQ31
PS_DDR_A0_502	DDR3 A0_3
PS_DDR_A1_502	DDR3 A1_3
PS_DDR_A2_502	DDR3 A2_3
PS_DDR_A3_502	DDR3 A3_3
PS_DDR_A4_502	DDR3 A4_3
PS_DDR_A5_502	DDR3 A5_3
PS_DDR_A6_502	DDR3 A6_3
PS_DDR_A7_502	DDR3 A7_3
PS_DDR_A8_502	DDR3 A8_3
PS_DDR_A9_502	DDR3 A9_3
PS_DDR_A10_502	DDR3 A10_3
PS_DDR_A11_502	DDR3 A11_3
PS_DDR_A12_502	DDR3 A12_3
PS_DDR_A13_502	DDR3 A13_3
PS_DDR_A14_502	DDR3 A14_3
PS_DDR_DQS_P0_502	DDR3 DQS0_3 P
PS_DDR_DQS_N0_502	DDR3 DQS0_3 N
PS_DDR_DQS_P1_502	DDR3 DQS1_3 P
PS_DDR_DQS_N1_502	DDR3 DQS1_3 N
PS_DDR_DQS_P2_502	DDR3 DQS2_3 P
PS_DDR_DQS_N2_502	DDR3 DQS2_3 N
PS_DDR_DQS_P3_502	DDR3 DQS3_3 P
PS_DDR_DQS_N3_502	DDR3 DQS3_3 N
PS_DDR_CK0_P_502	DDR3 CK0_3 P
PS_DDR_CK0_N_502	DDR3 CK0_3 N
PS_DDR_BA0_502	DDR3 BA0_3
PS_DDR_BA1_502	DDR3 BA1_3
PS_DDR_BA2_502	DDR3 BA2_3
PS_DDR_DM0_502	DDR3 DM0_3
PS_DDR_DM1_502	DDR3 DM1_3
PS_DDR_DM2_502	DDR3 DM2_3
PS_DDR_DM3_502	DDR3 DM3_3
PS_DDR_CS_B_502	DDR3 CS#_3
PS_DDR_WE_B_502	DDR3 WE#_3
PS_DDR_CAS_B_502	DDR3 CAS#_3
PS_DDR_RAS_B_502	DDR3 RAS#_3
PS_DDR_CKE_502	DDR3 CKE_3
PS_DDR_ODT_502	DDR3 ODT_3
PS_DDR_DRST_B_502	DDR3 RESET#_3
PS_DDR_VRP_502	
PS_DDR_VRN_502	

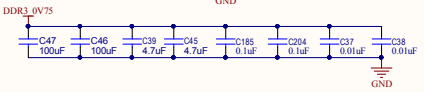
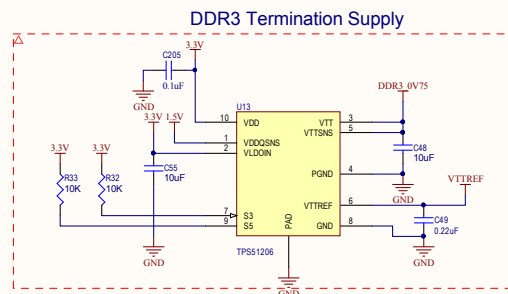
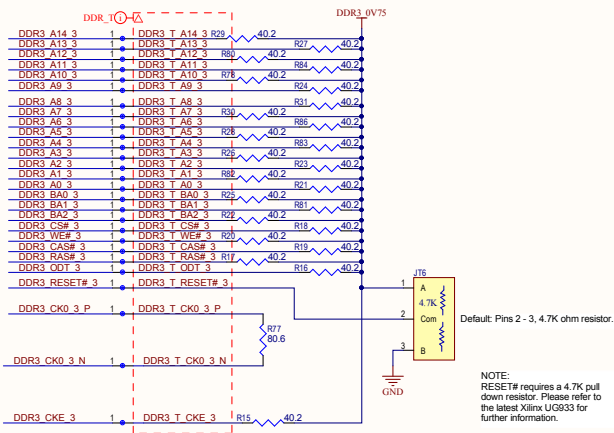
DDR_D_HL ○ DDR3 DQ[7..0]
 DDR_D_HL ○ DDR3 DQ[15..8]
 DDR_D_HL ○ DDR3 DQ[23..16]
 DDR_D_HL ○ DDR3 DQ[31..24]



Layout Note:
 DDR3 trace lengths must include Zynq package flight times. See UG933 and Layout Guidelines.

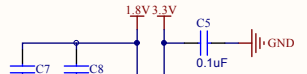
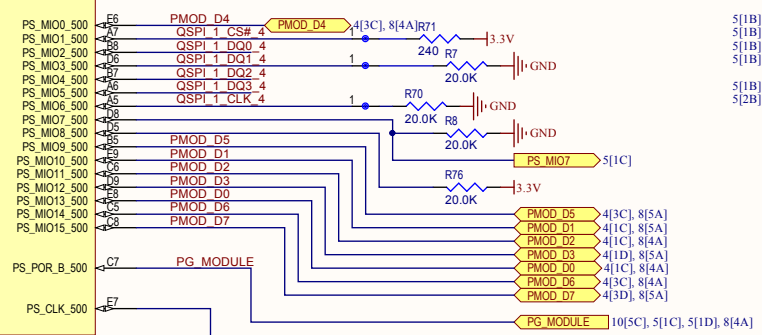
Layout Note:
 DDR3 target trace impedances are as follows:
 Single Ended Signals = 40 ohms
 Differential Signals = 80 ohms

Layout Note:
 Use Fly-by routing and termination for DDR3 control signals. Resistors should be placed past the last memory IC & as close to the device as possible.

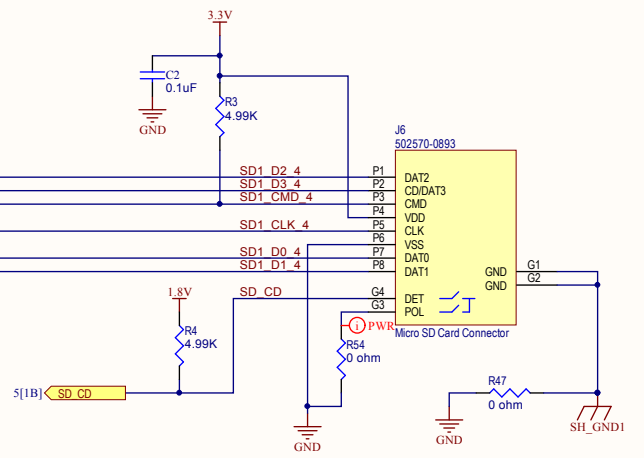


U9E
Zynq 7010/7020 SOC CLG400

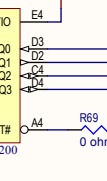
BANK 500



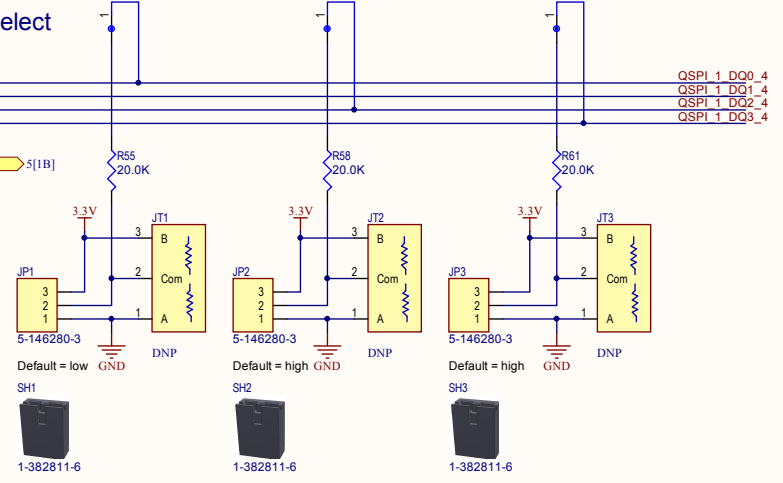
Micro SD Card



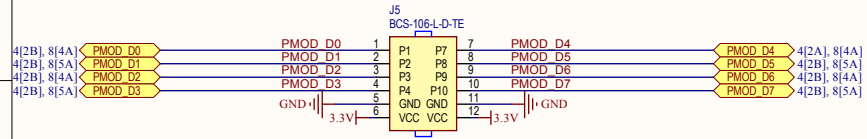
QSPI



Boot Mode Select

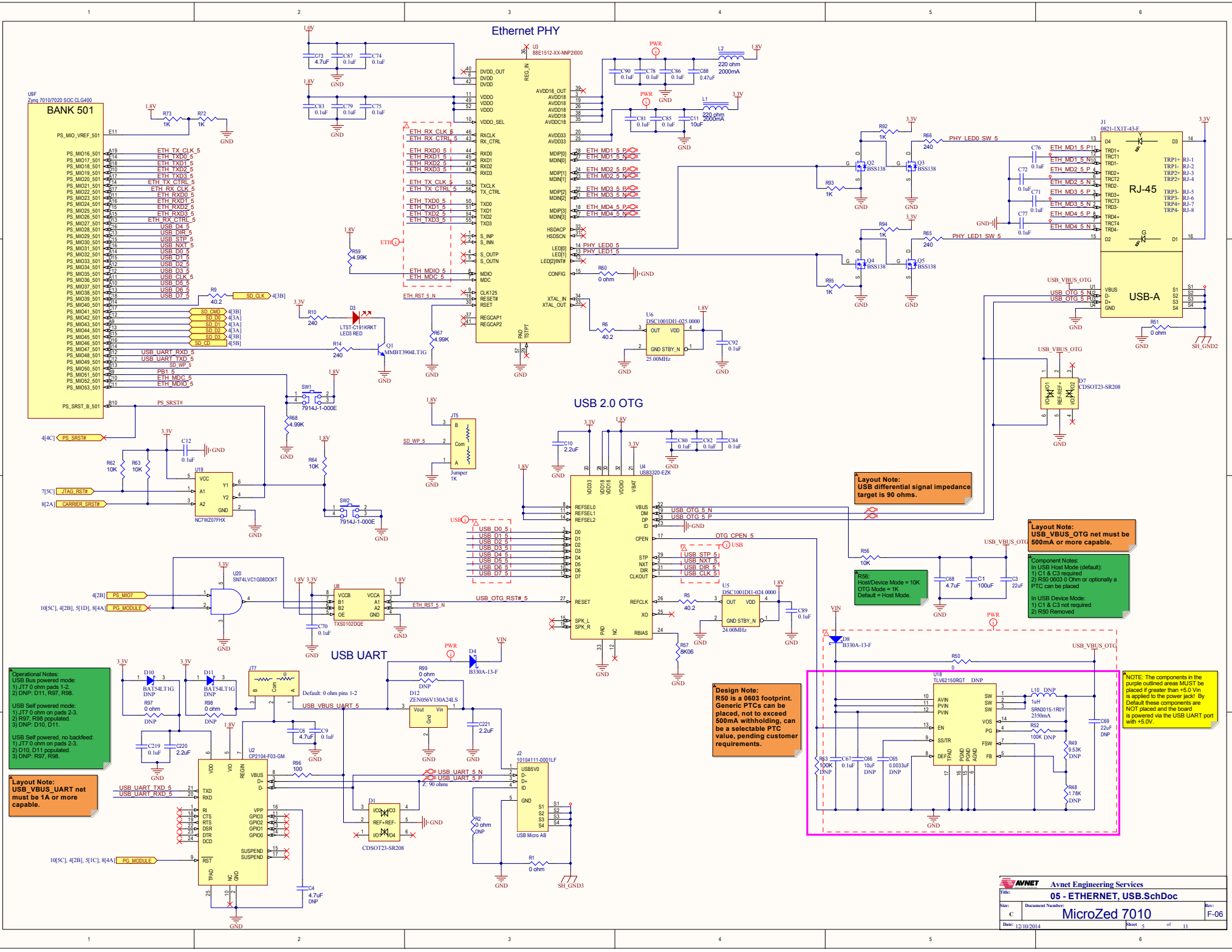


PMOD Interface



Boot Mode:	JT1:	JT2:	JT3:
Cascade JTAG	1-2 (low)	1-2 (low)	1-2 (low)
Ind. JTAG	2-3 (high)	2-3 (high)	2-3 (high)
QSPI	x	1-2 (low)	2-3 (high)
SD Card	1-2 (low)	2-3 (high)	2-3 (high)

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Title: 04 - QSPI FLASH, MicroSD.SchDoc
Size: B **Document Number:** **MicroZed 7010** **Rev:** F-06
Date: 12/10/2014 **Sheet 4** of 11



BANK 501
Zynq 7010/7020 SOC CL-G40

PS_M0_VREF_501	E11	1.8V
PS_M016_501	A19	ETH_TX_CLK_5
PS_M017_501	A14	ETH_TXD0_5
PS_M018_501	A18	ETH_TXD1_5
PS_M019_501	A10	ETH_TXD2_5
PS_M020_501	A17	ETH_TXD3_5
PS_M021_501	A14	ETH_TX_CTRL_5
PS_M022_501	A17	ETH_RX_CLK_5
PS_M023_501	A11	ETH_RXD0_5
PS_M024_501	A15	ETH_RXD1_5
PS_M025_501	A15	ETH_RXD2_5
PS_M026_501	A13	ETH_RXD3_5
PS_M027_501	A13	ETH_TX_CTRL_5
PS_M028_501	A16	USB_D4_5
PS_M029_501	A13	USB_DIR_5
PS_M030_501	A16	USB_NXT_5
PS_M031_501	A14	USB_OTG_5
PS_M032_501	A12	USB_D2_5
PS_M033_501	A14	USB_D3_5
PS_M034_501	A12	USB_D5_5
PS_M035_501	A11	USB_CLK_5
PS_M036_501	A10	USB_D6_5
PS_M037_501	A13	USB_D7_5
PS_M038_501	A18	USB_D8_5
PS_M039_501	A18	USB_D9_5
PS_M040_501	A17	SD_CLK_4(3B)
PS_M041_501	A12	SD_CMD_4(3B)
PS_M042_501	A12	SD_D0_4(3A)
PS_M043_501	A13	SD_D1_4(3A)
PS_M044_501	A13	SD_D2_4(3A)
PS_M045_501	A15	SD_D3_4(3B)
PS_M046_501	A14	SD_D4_4(3B)
PS_M047_501	A14	SD_D5_4(3B)
PS_M048_501	A12	USB_UART_RXD_5
PS_M049_501	A12	USB_UART_TXD_5
PS_M050_501	A13	USB_WP_5
PS_M051_501	A19	PBT_5
PS_M052_501	A11	ETH_MD0C_5
PS_M053_501	A11	ETH_MD10_5
PS_SRST#_501	B10	PS_SRST#

Operational Notes:
 USB Bus powered mode:
 1) J77 0 ohm pads 1-2
 2) DNP: D11, R97, R98.
 USB Self powered mode:
 1) J77 0 ohm on pads 2-3
 2) R97, R98 populated.
 3) DNP: D10, D11.
 USB Self powered, no backfeed:
 1) J77 0 ohm on pads 2-3
 2) D10, D11 populated.
 3) DNP: R97, R98.

Layout Note:
 USB_VBUS_UART not must be 1A or more capable.

Layout Note:
 USB differential signal impedance target is 90 ohms.

Layout Note:
 USB_VBUS_OTG net must be 500mA or more capable.

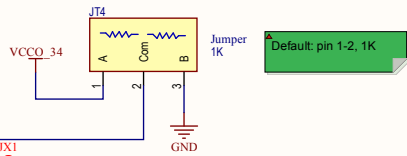
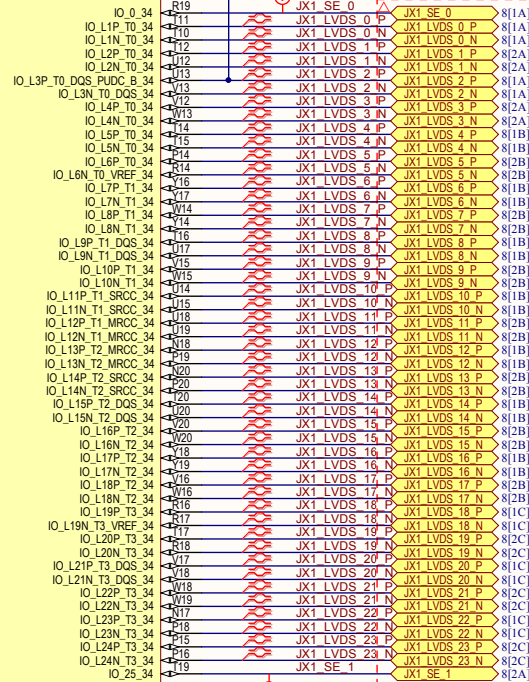
Component Notes:
 In USB Host Mode (default):
 1) C1 & C3 required
 2) R50 0603 0 Ohm or optionally a PTC can be placed.
 In USB Device Mode:
 1) C1 & C3 not required
 2) R50 Removed

Design Note:
 R50 is a 0603 footprint. Generic PTCs can be placed, not to exceed 500mA withstanding, can be a selectable PTC value, pending customer requirements.

NOTE: The components in the purple outlined areas MUST be placed if greater than +5.0V is applied to the power jack! By Default these components are NOT placed and the board is powered via the USB UART port with +5.0V.

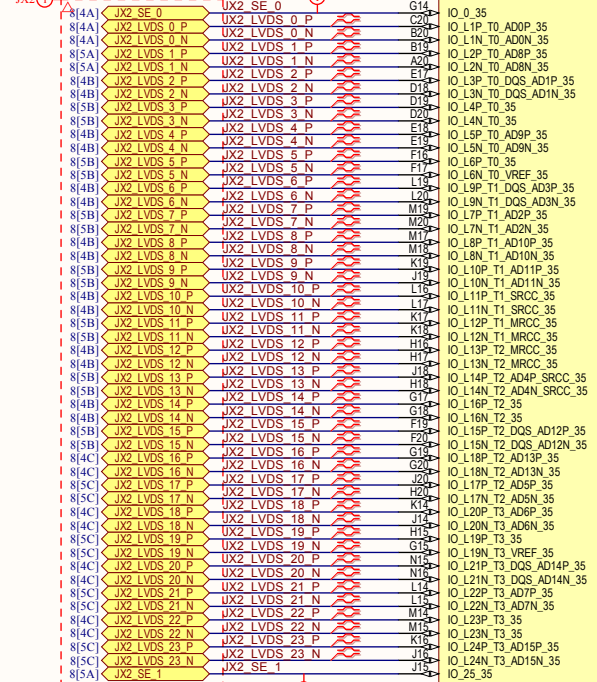
U9C
Zyma 7010/7020 SOC CLG400

BANK 34

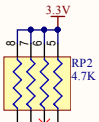
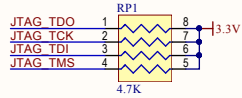
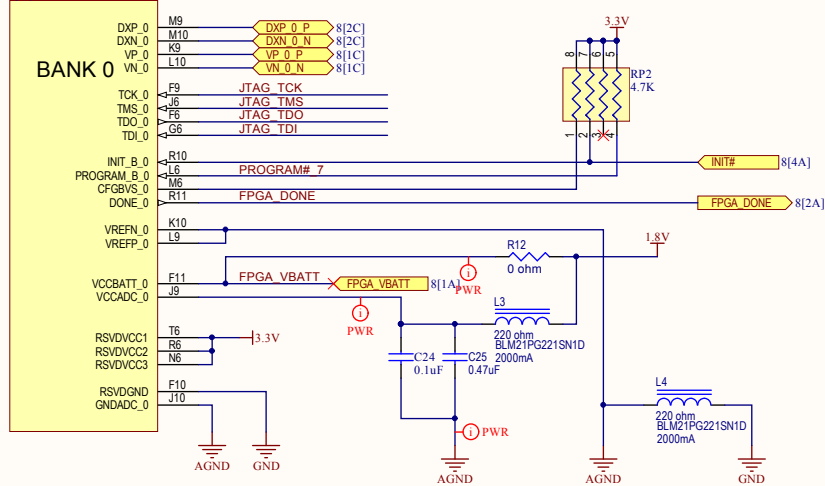


U9D
Zyma 7010/7020 SOC CLG400

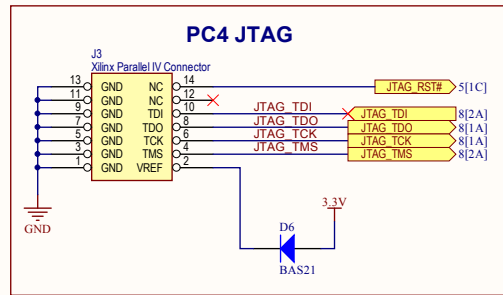
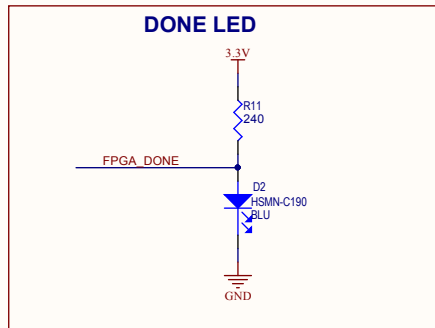
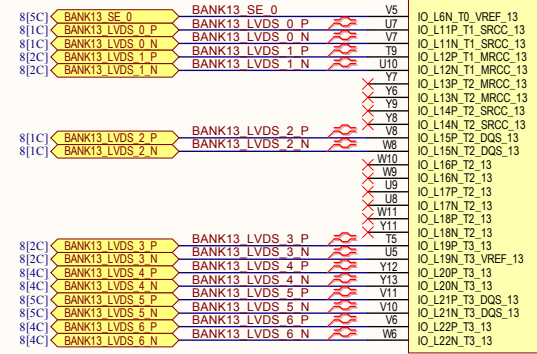
BANK 35



USA
Zyma 7010/7020 SOC CLG400



U9B
Zyma 7010/7020 SOC CLG400
**BANK 13
(Z7020 Only)**



1 2 3 4 5 6

A

B

C

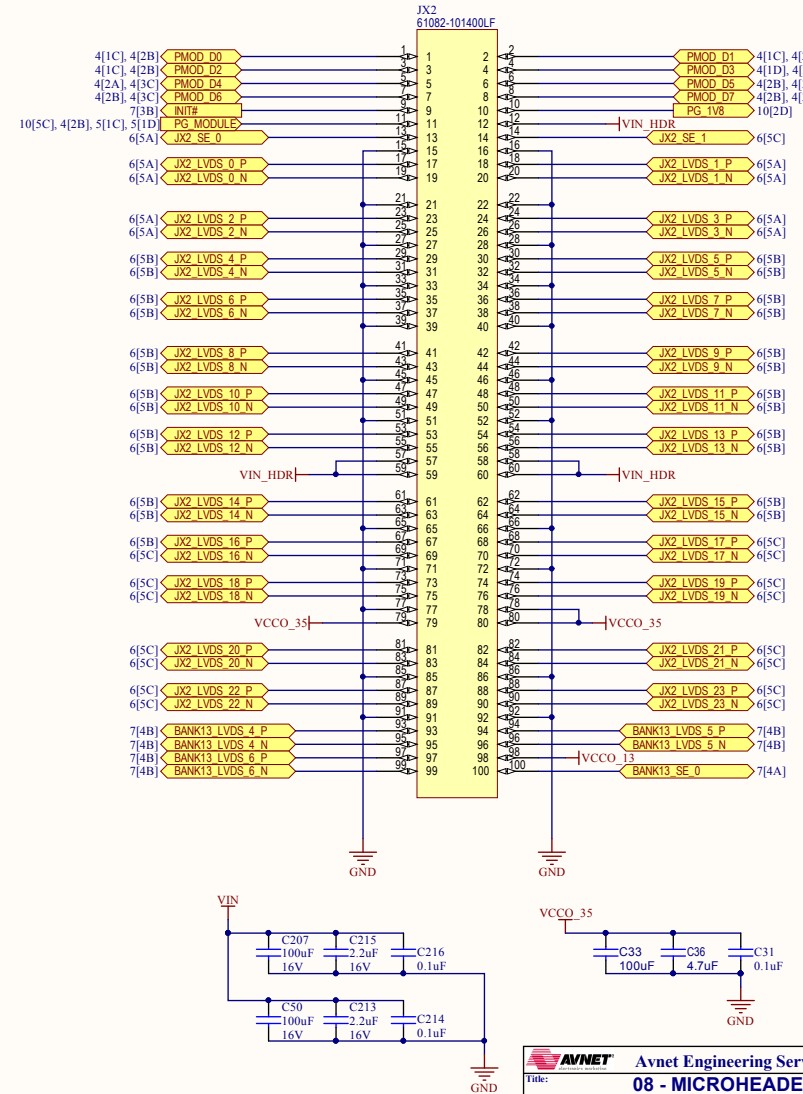
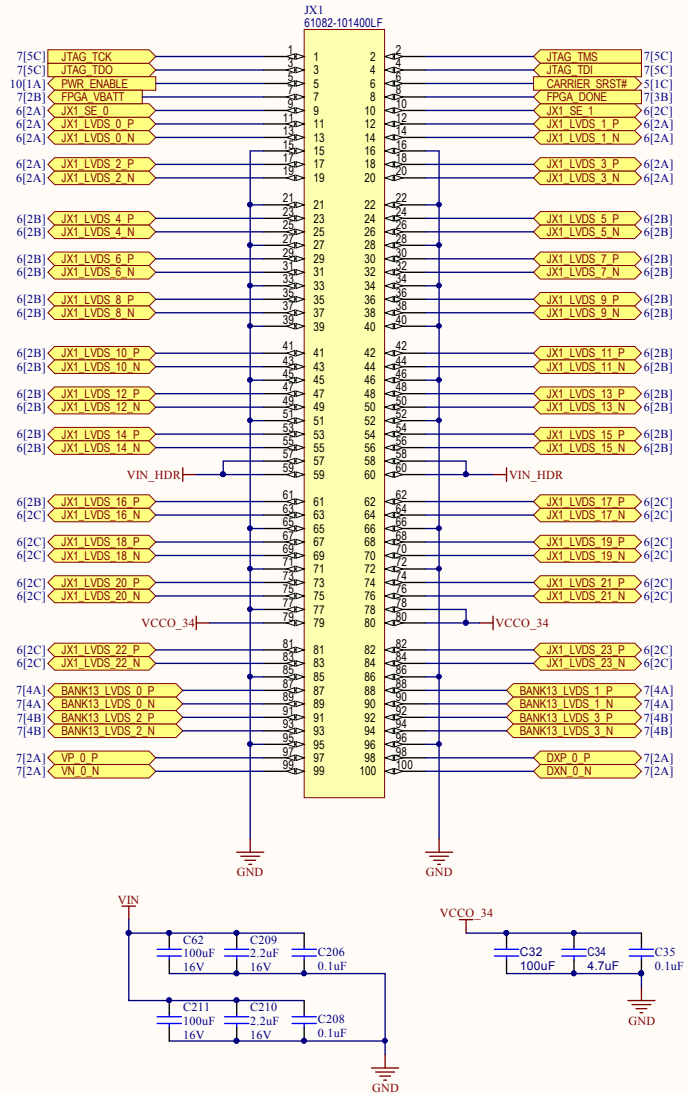
D

A

B

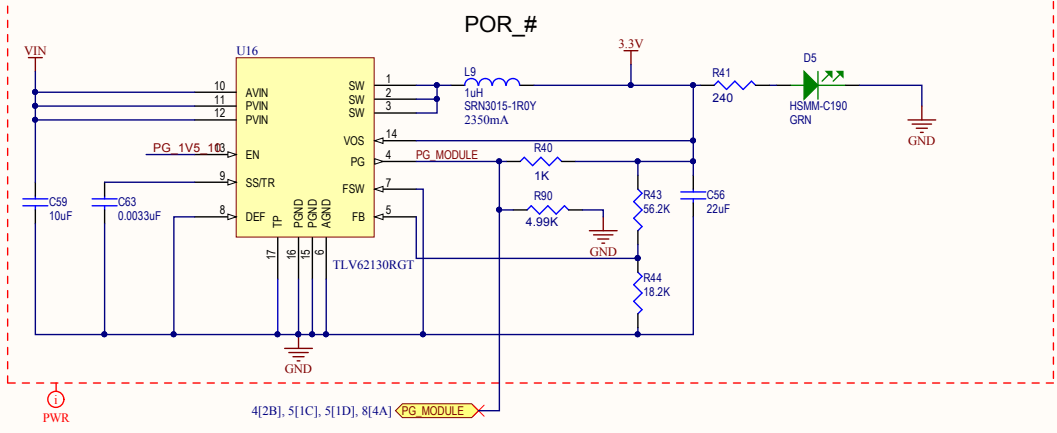
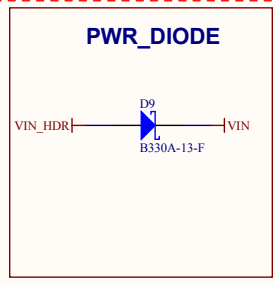
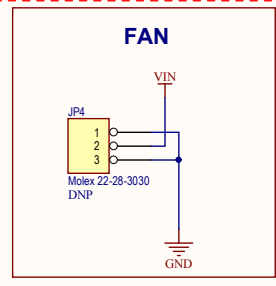
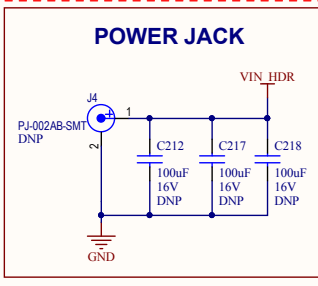
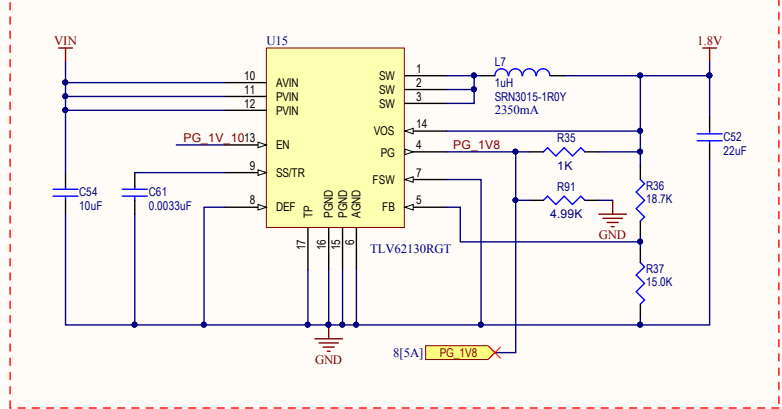
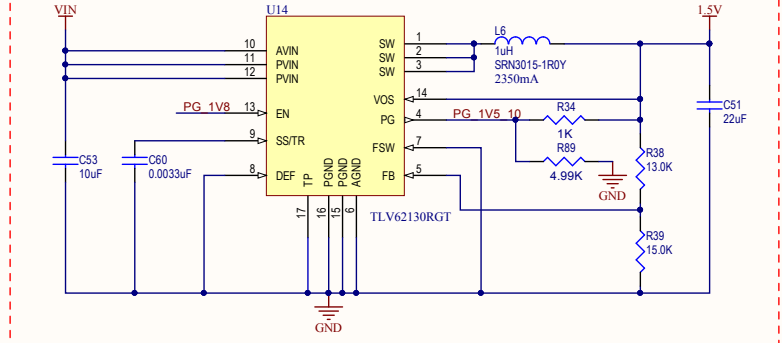
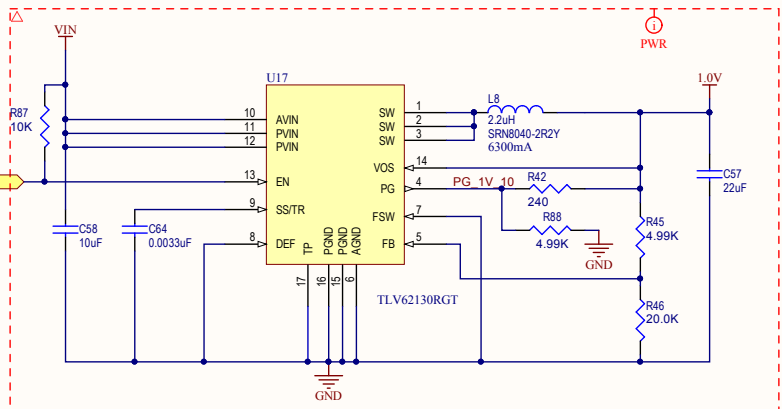
C

D



Avnet Engineering Services	
08 - MICROHEADERS.SchDoc	
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Size:	Document Number:
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Title: 10 - POWER, RESET.SchDoc	
Size: B	Document Number: MicroZed 7010
Date: 12/10/2014	Rev: F-06

Revision Notes:

Revision C Changes:

- 1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
- 2) Reduce R34, 35, (40), 42 from 100K to 1K
- 3) Add pulldown resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
- 4) Fuse (PTC) recommendation note for R50, 12V input
- 5) Connect: U8.6 to U20.2
- 6) Connect: U3.16 to U8.3
- 7) Connect: JX2.10 to U15.4
- 8) Change 4.75K resistors to 4.99K
- 9) Added rubber feet to BOM
- 10) Add staple point vias for J2 USB connector.

Revision D Changes (no production):

- 1) Attached JX2.10 to U15.4

Revision E Changes (no production):

- 1) Replaced U11 from MAX13035EETE+ to TI TXS02612ZQSR part.
- 2) Added Sheet 11.
- 3) Moved mechanical information to back page.

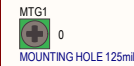
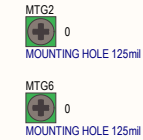
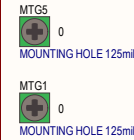
Revision F Changes:

- 1) Changed USB UART default power to bus power. Attach VBUS power net to U2.7 REGIN pin. Disconnect Vdd pin from +3.3V.
- 2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
- 3) Added: D10, D11, J17, R97, R98 to allow user to configure USB Bus or Self power mode.
- 4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
- 5) Added D12 PolyZen (PTC+Zen) USB UART protection component as configurable option.
- 6) Added R99 0 ohm resistor for D12 bypass (default).
- 7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
- 8) Revised notes (above).
- 9) 28 Jan 14: Updated USB OTG configuration notes.
- 10) 32F ge'36-Updated J16 note'up'ij ggv'5.

Mechanicals:




PCB Mounting Holes



Fansink Mounting Holes



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